SHARP

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Page Mode Dual Work Flash Memory

32M-bit, 64M-bit, 128M-bit

LH28F320BF, LH28F640BF, LH28F128BF Series

Appendix

Rev. F

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  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliance
  - Communication equipment other than for trunk lines

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  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

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  - Communications equipment for trunk lines
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  - Medical equipment related to life support, etc.

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1 Introduction

This appendix describes how to use the LH28F320BF series, LH28F640BF series and LH28F128BF series, Page Mode Dual Work Flash memory. In this document, all the functions for the LH28F320BF series, LH28F640BF series and LH28F128BF series are explained. However, the function which is available varies according to each product. Refer to the specifications whether each function in this document is available or not. The function which is not described in the specifications can not be used for that product.

The LH28F320BF series, LH28F640BF series and LH28F128BF series Flash memory are called the product in this document.

Section 1 outlines the product. Sections 2, 3, 4 and 5 describe the memory organization and functionality. When designing a specific system, take into design considerations described in Section 5.

1.1 Features

The product has the following features:

- Dual work operation
- Flexible partition configuration
- High performance asynchronous reads
- Page buffer program
- Individual block locking and all blocks locked on power-up
- 8-word OTP (One Time Program) block
- Low power consumption
- Parameter block architecture

1.2 Definition of Block, Plane and Partition

Block, Plane and Partition are defined and used in this document as explained below. Refer to the specifications for the number of blocks, planes and partitions of the product which has two or more BE# (CE#) pins or which has 32-bit I/O interface.

- Block
  Main Block: 32K Words.
  Parameter Block: 4K Words.
  32M-bit device has 8 parameter blocks and 63 main blocks.
  64M-bit device has 8 parameter blocks and 127 main blocks.
- Plane: 32M-bit and 64M-bit devices are divided into four physical planes (see Table 1). Plane0 or Plane3 contains parameter blocks and main blocks. Plane1 and Plane2 consist of only main blocks.
- Partition: Read operation can be done in one partition while Program/Erase operation is being done in another partition. Partition contains at least one plane or up to four planes. Partition boundaries can be flexibly set to any plane boundary by the Set Partition Configuration Register command. If the partition configuration register is set to "111" (4 plane dual work mode), the partition is exactly the same as a plane. See Section 4.17 for more information.

Table 1. Address Range of Each Plane (1), (2)

Plane #	Contains the Blocks within the following Address	
	32M bit	64M bit
Plane 0	000000H-07FFFFH	000000H-0FFFFFH
Plane 1	080000H-0FFFFFH	100000H-1FFFFFH
Plane 2	100000H-17FFFFH	200000H-2FFFFFH
Plane 3	180000H-1FFFFFH	300000H-3FFFFFH

NOTE:
1. This table shows the density of memory area selected by each BE# (CE#) when the product has two or more BE# (CE#) pins
2. Refer to the specifications for the address range of the product which has 32-bit I/O interface.

1.3 Product Overview

The product is capable of dual work operation: erase or program operation on one partition and read operation on other partitions (see Table 2). The partition to be accessed is automatically identified according to the input address. Dual work operations can be achieved by dividing the memory array into four physical planes as shown in Figure 2.1 through Figure 3.2. Each plane is exactly one quarter of the entire memory array. The device has also virtual partitions. Several planes can be flexibly merged to one partition by writing the Set Partition Configuration Register command. This feature allows the user to read from one partition even though one of the other partitions is executing an erase or program operation. If the device is set to the 4 partitions configuration, each partition is exactly the same as each physical plane. After power-up or device reset, plane 0-2 are merged into one partition for top parameter devices and plane1-3 are merged into one partition for bottom parameter devices.

During dual work operation, read operations to the partition being erased or programmed access the status register which indicates whether the erase or program operation is successfully completed or not. Dual work operation cannot be executed during full chip erase and OTP program mode.

Memory array data can be read in asynchronous 8-word page mode. The default after power-up or device reset is the asynchronous read mode in which 8-word page mode is available.

The product contains a page buffer of 16 words. In the page buffer program mode, the data to be programmed is first stored into the page buffer before being transferred to the memory array. A page buffer program has high speed program performance. The page buffer program operation programs up to 16-word data at sequential addresses within one block. That is, this operation cannot be used to program data at addresses separated by something even in the same block, or divided into different blocks. Page buffer program cannot be applied to OTP block described later in this section.

For the parameter blocks and main blocks, individual block locking scheme that allows any block to be locked, unlocked or locked-down with no latency. The time required for block locking is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#). The block is locked via the Set Block Lock Bit command or Set Block Lock-down bit command. Block erase, full chip erase and (page buffer) program operation cannot be executed for locked block, to protect codes and data from unwanted operation due to noises, etc. When the WP# pin is at V_{IL}, the locked-down block cannot be unlocked. When WP# pin is at V_{IH}, lock-down bits are disabled and any block can be locked or unlocked through software. After WP# goes V_{IL}, any block previously marked lock-down revert to that state. At power-up or device reset, all blocks default to locked state and are not locked-down, regardless of the states before power-off or reset operation. This means that all write operations on any block are disabled.

Unauthorized use of cellular phone, communication device, etc. can be avoided by storing a security code into the 8-word OTP (One Time Program) block (see Figure 4) provided in addition to the parameter and main blocks. To ensure high reliability, a lock function for the OTP block is provided.

The product has a V_{PP} pin which monitors the level of the power supply voltage. When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered and the data in all blocks are completely write protected (see Note 1). Note that the V_{PP} is used only for checking the supply voltage, not used for device power supply pin.

Automatic Power Savings (APS) is the low power features to help increase battery life in portable applications. APS mode is initiated shortly after read cycle completion. In this mode, its current consumption decreases to the value equivalent of that in the standby mode. Standard address access timings (t_{AVQV}) provide new data when addresses are changed. During dual work operation (one partition being erased or programmed, while other partitions are read modes), the device cannot enter the Automatic Power savings mode if the input address remains unchanged.

A CUI (Command User Interface) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. The product uses an advanced WSM (Write State Machine) to automatically execute erase and program operations within the memory array. The WSM is controlled through the CUI. By writing a valid command sequence to the CUI, the WSM is instructed to automatically handle the sequence of internal events and timings required to block erase, full chip erase, (page buffer) program or OTP program operations.

Status registers are prepared for each partition to indicate the status of the partition. Even if the WSM is occupied by executing erase or program operation in one partition, the status register of other partition reports that the device is not busy when the device is set to 2, 3 or 4 partitions configuration.

(Note 1) Please note following:

- For the lockout voltage V_{PPLK} to inhibit all write functions, refer to specifications.
- V_{PP} should be kept lower than V_{PPLK} (GND) during read operations to protect the data in all blocks.

When the RST# pin is at V_{IL}, reset mode is enabled which minimizes power consumption and provides write protection. The RST# is also useful for resetting the WSM to read array mode and initializing the status register bits to "80H". During power-on/off or transitions, keep the RST# pin at V_{IL} level to protect the data from noises, and initialize the device's internal control circuit.

A reset time (t_{PHQV}) is required from RST# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHWL}, t_{PHEL}) from RST#-high until writes to the CUI are recognized.

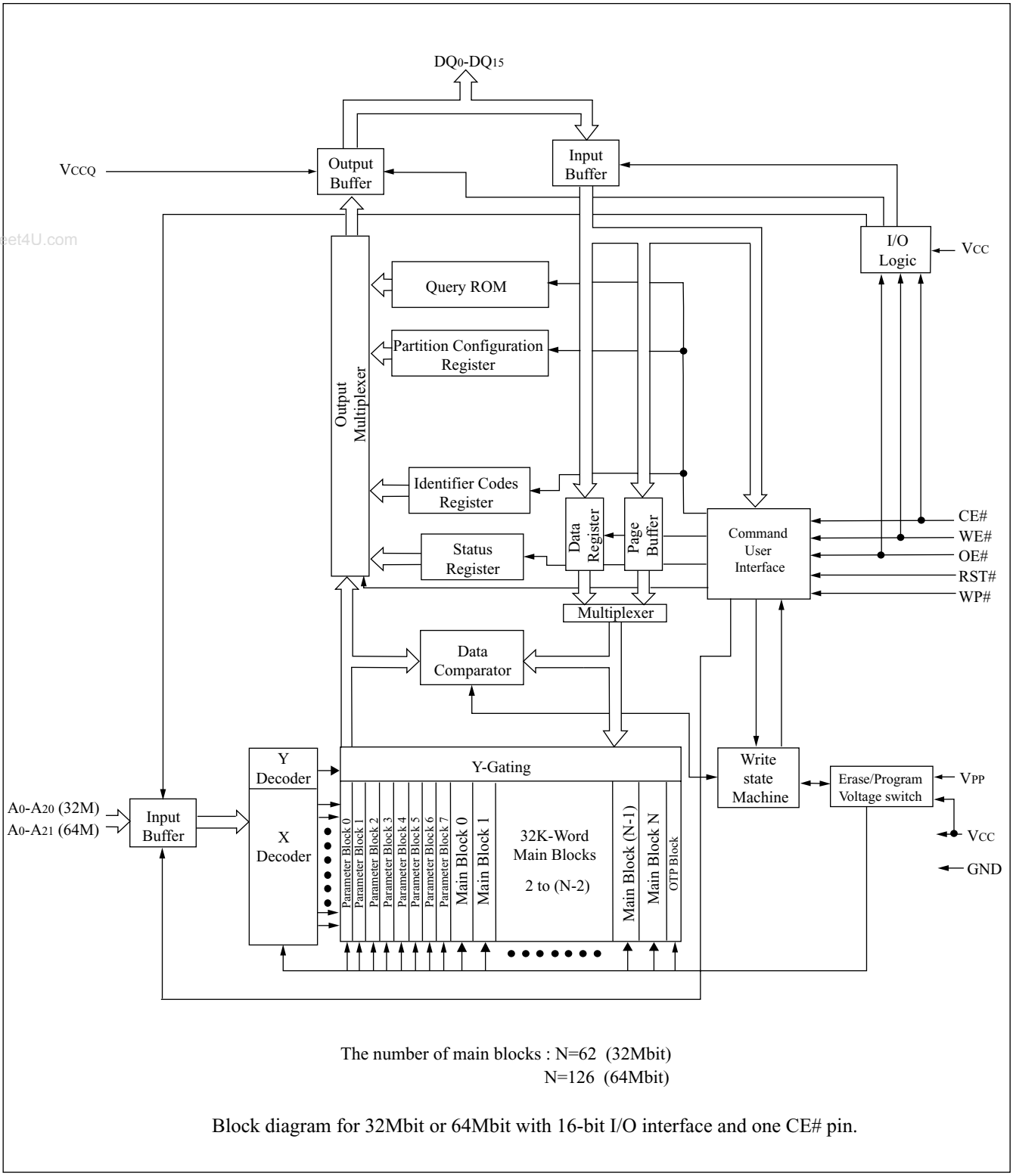
Erase operation erases one block or all blocks. Programming is executed in either one word increments or by page sized increments using the high speed program page buffers. These operations use an industry standard set of CUI command sequences. Suspend commands exist for both the erase and program operations to permit the system to interrupt an erase or program operation in progress to enable the access to another memory location in the same partition. Nested suspend is also supported. This allows the software to suspend an erase in one partition, start programming in a second partition, suspend programming in the second partition, then read from the second partition. After reading from the second partition, resume the suspended program in the second partition, then resume the suspended erase in the first partition.

Figure 1 shows the block diagram for the product. The example of pin descriptions are explained in Table 3.

Table 2. Simultaneous Operation Modes Allowed with Four Planes(1, 2)

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:
1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.



The number of main blocks : N=62 (32Mbit)
N=126 (64Mbit)

Block diagram for 32Mbit or 64Mbit with 16-bit I/O interface and one CE# pin.

Figure 1. Block Diagram

Table 3. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses. 32M: A_0-A_{20}
A_0-A_{21}	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M or 128M: A_0-A_{21}
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V_{IL}), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP# is V_{IH}, lock-down is disabled.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM (Write State Machine). When low, WSM is performing an internal operation (block erase, full chip erase, (page buffer) program or OTP program). RY/BY#-High Z indicates that the WSM is ready for new commands, block erase is suspended and (page buffer) program is inactive, (page buffer) program is suspended, or the device is in reset mode.
V_{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pin. With $V_{PP} \le V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (see specifications): With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (see specifications): Power supply for all input/ output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

1.4 Product Description

1.4.1 Memory Block Organization

The device is divided into four physical planes and the partitions can be flexibly configured by the Set Partition Configuration Register command. This allows dual work operations, that is, simultaneous read-while-erase and read-while-program operations. For the address locations of the blocks, see the memory map in Figure 2.1 through Figure 3.2.

Refer to the specifications for the address locations of the product which has two or more BE# (CE#) pins or which has 32-bit I/O interface.

1.4.2 Four Physical Planes

The product has four physical planes (one parameter plane and three uniform planes). Each plane consists of 8M-bit (32M-bit device) or 16M-bit (64M-bit device) Flash memory. The parameter plane consists of eight 4K-word parameter blocks and fifteen (32M-bit device) or thirty-one (64M-bit device) 32K-word main blocks. Each uniform plane consists of sixteen (32M-bit device) or thirty-two (64M-bit device) 32K-word main blocks. Each block can be erased independently up to 100,000 times.

Refer to the specifications for the number of planes and each plane density of the product which has two or more BE# (CE#) pins or which has 32-bit I/O interface.

1.4.3 Partition

Partition boundaries can be configured by the Set Partition Configuration Register command. Dual work operation can be done in two partitions. See partition configuration in Table 14 and Figure 15 for more detail. Only one partition can be erased or programmed at a time. Simultaneous operation modes are shown in Table 2.

1.4.4 Parameter Block

Eight 4K-word parameter blocks within the parameter partition are provided as the memory area to facilitate storage of frequently update small parameters that would normally be stored in EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. The protection of the parameter block is controlled using a combination of the V_{PP}, RST#, WP#, block lock bit and block lock-down bit.

1.4.5 Main Block

32K-word main blocks can store code and/or data. The protection of the main block is also controlled using a combination of the V_{PP}, RST#, WP#, block lock bit and block lock-down bit.

1.4.6 OTP (One Time Program) block

The OTP block is a special block that cannot be erased in order to secure the high system reliability. This 8-word (128-bit) OTP block is independent of main blocks and parameter blocks. Figure 4 shows the OTP block address map.

The OTP block is divided into two areas. One is a factory programmed area where a unique number has been programmed in SHARP factory. This factory programmed area is "READ ONLY" (already locked). The other is a customer programmable area that can be available for customers. This customer programmable area can also be locked. After locking, this customer programmable area is protected permanently.

The data within the OTP block can be read by the Read Identifier Codes/OTP command (90H). To return to read array mode, write the Read Array command (FFH) to the CUI.

The OTP block bits are programmed by writing the OTP Program command (C0H) to the CUI. Write the OTP Program command (C0H) at the 1st command cycle and then write the address and the data at the 2nd cycle. If the OTP program operation is failed, the status register bit SR.4 is set to "1". If the OTP block is locked, the status register bits SR.4 and SR.1 are set to "1".

The OTP block can be locked using the OTP Program command (C0H). Write the OTP Program command (C0H) at the 1st command cycle and then write the data (FFFDH) to the lock location (80H) at the 2nd cycle. Read cycle from address (80H) indicates the lockout state of the OTP block. Bit 0 of address (80H) means the factory programmed area lock state ("1" is "NOT LOCKED" and "0" is "LOCKED"). Bit 1 of address (80H) means the customer programmable lock state. OTP block lockout state is not reversible. Unlike the main array block lock configuration, the lock state of the OTP block is kept unchanged even if the power is turned off or reset operation is performed.

The OTP Program command is only available for programming the OTP block. Page buffer program operations are available for the main array. OTP program cannot be suspended through the (Page Buffer) Program Suspend command (described later). Dual work operation cannot be executed during OTP program.

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (PARAMETER PLANE)	70	4K-WORD	1FF000H - 1FFFFFH
	69	4K-WORD	1FE000H - 1FEFFFH
	68	4K-WORD	1FD000H - 1FDFFFH
	67	4K-WORD	1FC000H - 1FCFFFH
	66	4K-WORD	1FB000H - 1FBFFFH
	65	4K-WORD	1FA000H - 1FAFFFH
	64	4K-WORD	1F9000H - 1F9FFFH
	63	4K-WORD	1F8000H - 1F8FFFH
	62	32K-WORD	1F0000H - 1F7FFFH
	61	32K-WORD	1E8000H - 1EFFFFH
	60	32K-WORD	1E0000H - 1E7FFFH
	59	32K-WORD	1D8000H - 1DFFFFH
	58	32K-WORD	1D0000H - 1D7FFFH
	57	32K-WORD	1C8000H - 1CFFFFH
	56	32K-WORD	1C0000H - 1C7FFFH
	55	32K-WORD	1B8000H - 1BFFFFH
	54	32K-WORD	1B0000H - 1B7FFFH
	53	32K-WORD	1A8000H - 1AFFFFH
	52	32K-WORD	1A0000H - 1A7FFFH
	51	32K-WORD	198000H - 19FFFFH
	50	32K-WORD	190000H - 197FFFH
	49	32K-WORD	188000H - 18FFFFH
	48	32K-WORD	180000H - 187FFFH
PLANE2 (UNIFORM PLANE)	47	32K-WORD	178000H - 17FFFFH
	46	32K-WORD	170000H - 177FFFH
	45	32K-WORD	168000H - 16FFFFH
	44	32K-WORD	160000H - 167FFFH
	43	32K-WORD	158000H - 15FFFFH
	42	32K-WORD	150000H - 157FFFH
	41	32K-WORD	148000H - 14FFFFH
	40	32K-WORD	140000H - 147FFFH
	39	32K-WORD	138000H - 13FFFFH
	38	32K-WORD	130000H - 137FFFH
	37	32K-WORD	128000H - 12FFFFH
	36	32K-WORD	120000H - 127FFFH
	35	32K-WORD	118000H - 11FFFFH
	34	32K-WORD	110000H - 117FFFH
	33	32K-WORD	108000H - 10FFFFH
	32	32K-WORD	100000H - 107FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	31	32K-WORD	0F8000H - 0FFFFFH
	30	32K-WORD	0F0000H - 0F7FFFH
	29	32K-WORD	0E8000H - 0EFFFFH
	28	32K-WORD	0E0000H - 0E7FFFH
	27	32K-WORD	0D8000H - 0DFFFFH
	26	32K-WORD	0D0000H - 0D7FFFH
	25	32K-WORD	0C8000H - 0CFFFFH
	24	32K-WORD	0C0000H - 0C7FFFH
	23	32K-WORD	0B8000H - 0BFFFFH
	22	32K-WORD	0B0000H - 0B7FFFH
	21	32K-WORD	0A8000H - 0AFFFFH
	20	32K-WORD	0A0000H - 0A7FFFH
	19	32K-WORD	098000H - 09FFFFH
	18	32K-WORD	090000H - 097FFFH
	17	32K-WORD	088000H - 08FFFFH
	16	32K-WORD	080000H - 087FFFH
PLANE0 (UNIFORM PLANE)	15	32K-WORD	078000H - 07FFFFH
	14	32K-WORD	070000H - 077FFFH
	13	32K-WORD	068000H - 06FFFFH
	12	32K-WORD	060000H - 067FFFH
	11	32K-WORD	058000H - 05FFFFH
	10	32K-WORD	050000H - 057FFFH
	9	32K-WORD	048000H - 04FFFFH
	8	32K-WORD	040000H - 047FFFH
	7	32K-WORD	038000H - 03FFFFH
	6	32K-WORD	030000H - 037FFFH
	5	32K-WORD	028000H - 02FFFFH
	4	32K-WORD	020000H - 027FFFH
	3	32K-WORD	018000H - 01FFFFH
	2	32K-WORD	010000H - 017FFFH
	1	32K-WORD	008000H - 00FFFFH
	0	32K-WORD	000000H - 007FFFH

Figure 2.1. Memory Map for 32Mbit (Top Parameter)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
PLANE2 (UNIFORM PLANE)	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
	39	32K-WORD	100000H - 107FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	38	32K-WORD	0F8000H - 0FFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
PLANE0 (PARAMETER PLANE)	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
	7	4K-WORD	007000H - 007FFFH
	6	4K-WORD	006000H - 006FFFH
	5	4K-WORD	005000H - 005FFFH
	4	4K-WORD	004000H - 004FFFH
	3	4K-WORD	003000H - 003FFFH
	2	4K-WORD	002000H - 002FFFH
	1	4K-WORD	001000H - 001FFFH
	0	4K-WORD	000000H - 000FFFH

Figure 2.2. Memory Map for 32Mbit (Bottom Parameter)

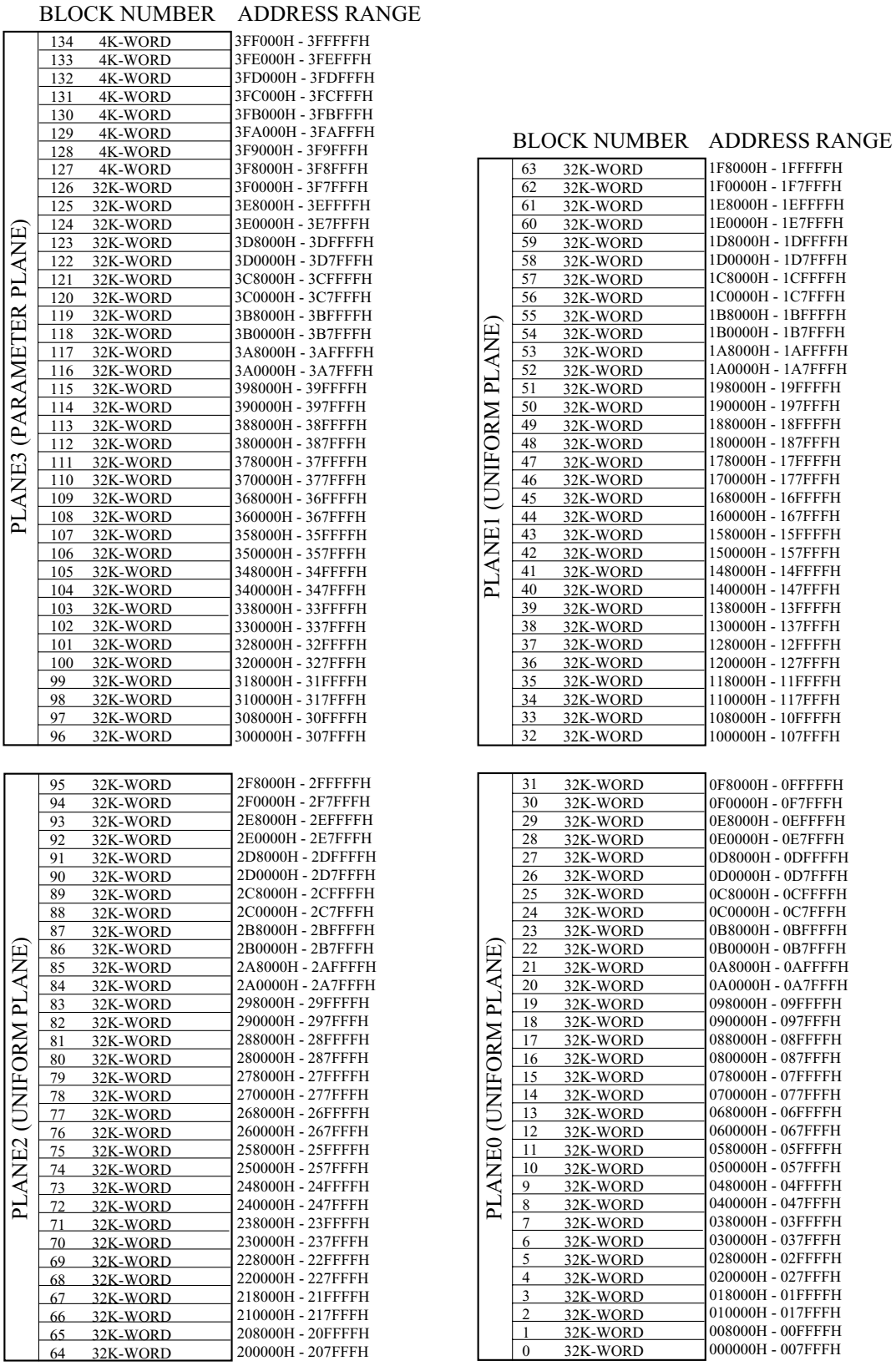


Figure 3.1. Memory Map for 64Mbit (Top Parameter)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	134	32K-WORD	3F8000H - 3FFFFFH
	133	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127	32K-WORD	3C0000H - 3C7FFFH
	126	32K-WORD	3B8000H - 3BFFFFH
	125	32K-WORD	3B0000H - 3B7FFFH
	124	32K-WORD	3A8000H - 3AFFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
	122	32K-WORD	398000H - 39FFFFH
	121	32K-WORD	390000H - 397FFFH
	120	32K-WORD	388000H - 38FFFFH
	119	32K-WORD	380000H - 387FFFH
	118	32K-WORD	378000H - 37FFFFH
	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
	115	32K-WORD	360000H - 367FFFH
	114	32K-WORD	358000H - 35FFFFH
	113	32K-WORD	350000H - 357FFFH
	112	32K-WORD	348000H - 34FFFFH
	111	32K-WORD	340000H - 347FFFH
	110	32K-WORD	338000H - 33FFFFH
	109	32K-WORD	330000H - 337FFFH
	108	32K-WORD	328000H - 32FFFFH
	107	32K-WORD	320000H - 327FFFH
	106	32K-WORD	318000H - 31FFFFH
	105	32K-WORD	310000H - 317FFFH
	104	32K-WORD	308000H - 30FFFFH
	103	32K-WORD	300000H - 307FFFH

PLANE2 (UNIFORM PLANE)	102	32K-WORD	2F8000H - 2FFFFFH
	101	32K-WORD	2F0000H - 2F7FFFH
	100	32K-WORD	2E8000H - 2EFFFFH
	99	32K-WORD	2E0000H - 2E7FFFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
	93	32K-WORD	2B0000H - 2B7FFFH
	92	32K-WORD	2A8000H - 2AFFFFH
	91	32K-WORD	2A0000H - 2A7FFFH
	90	32K-WORD	298000H - 29FFFFH
	89	32K-WORD	290000H - 297FFFH
	88	32K-WORD	288000H - 28FFFFH
	87	32K-WORD	280000H - 287FFFH
	86	32K-WORD	278000H - 27FFFFH
	85	32K-WORD	270000H - 277FFFH
	84	32K-WORD	268000H - 26FFFFH
	83	32K-WORD	260000H - 267FFFH
	82	32K-WORD	258000H - 25FFFFH
	81	32K-WORD	250000H - 257FFFH
	80	32K-WORD	248000H - 24FFFFH
	79	32K-WORD	240000H - 247FFFH
	78	32K-WORD	238000H - 23FFFFH
	77	32K-WORD	230000H - 237FFFH
	76	32K-WORD	228000H - 22FFFFH
	75	32K-WORD	220000H - 227FFFH
	74	32K-WORD	218000H - 21FFFFH
	73	32K-WORD	210000H - 217FFFH
	72	32K-WORD	208000H - 20FFFFH
	71	32K-WORD	200000H - 207FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
	39	32K-WORD	100000H - 107FFFH

PLANE0 (PARAMETER PLANE)	38	32K-WORD	0F8000H - 0FFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
	7	4K-WORD	007000H - 007FFFH
	6	4K-WORD	006000H - 006FFFH
	5	4K-WORD	005000H - 005FFFH
	4	4K-WORD	004000H - 004FFFH
	3	4K-WORD	003000H - 003FFFH
	2	4K-WORD	002000H - 002FFFH
	1	4K-WORD	001000H - 001FFFH
	0	4K-WORD	000000H - 000FFFH

Figure 3.2. Memory Map for 64Mbit (Bottom Parameter)

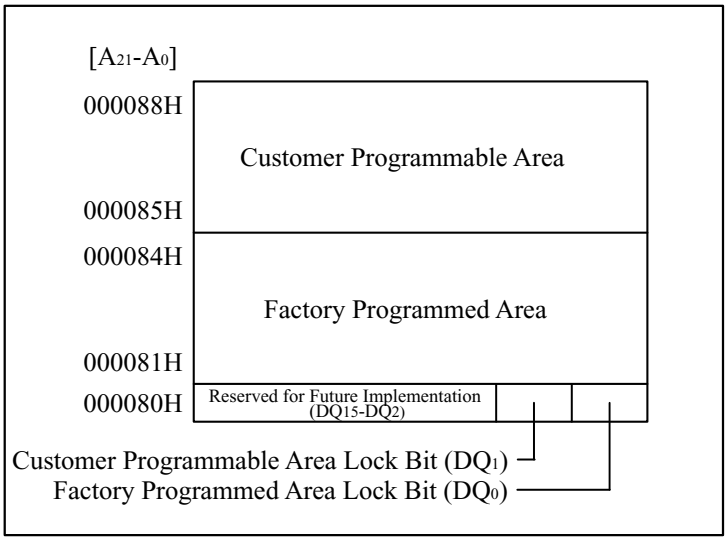


Figure 4. OTP Block Address Map for OTP Program(1, 2)
(The area outside 80H~88H cannot be used.)

NOTES:
1. A_{21} is not used for 32M-bit device.
2. Refer to Table 6 through Table 8 as to the OTP block address map for read operation.

2 Principles of Operation

The product includes an on-chip WSM (Write State Machine) and can automatically execute block erase, full chip erase, (page buffer) program or OTP program operation after writing the proper command to the CUI (Command User Interface).

2.1 Operation Mode after Power-up or Reset Mode

After initial power-up or reset mode (refer to Bus Operation in Section 3), the device defaults to the following mode.

- Asynchronous read mode in which 8-word page mode is available
- Plane 0-2 are merged into one partition for top parameter devices and plane1-3 are merged into one partition for bottom parameter devices.
- All blocks default to locked state and are not locked-down.

Manipulation of external memory control pins (CE#, OE#) allow read array, standby and output disable modes.

2.2 Read, Program and Erase Operation

Independent of the V_{PP} voltage, the memory array, status register, identifier codes, OTP block and query codes can be accessed. And also, set/clear block lock configuration and set partition configuration register are available even if the V_{PP} voltage is lower than V_{PPLK}. Applying the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP} enables successful block erase, (page buffer) program and OTP program operation. Applying the specified voltage on V_{CC} and V_{PPH1} on V_{PP} enables successful full chip erase operation. All functions associated with altering memory contents, which is block erase, full chip erase, (page buffer) program and OTP program, are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. Addresses and data are internally latched on the rising edge of CE# or WE# whichever goes high first during command write cycles. The CUI contents serve as input to the WSM, which controls block erase, full chip erase, (page buffer) program and OTP program. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Writing the appropriate command outputs array data, status register data, identifier codes, lock configuration codes, device configuration codes, data within the OTP block and query codes.

In any block, the user can store an interface software that initiates and polls progress of block erase or (page buffer) program. Because the product has dual work function, data can be read from the partition not being erased or programmed without using the block erase suspend or (page buffer) program suspend. When the target partition is being erased or programmed, block erase suspend or (page buffer) program suspend allows system software to read/program data from/to blocks other than that which is suspended.

2.3 Status Register for Each Partition

The product has status registers for each partition. The 8-bit status register is available to monitor the partition state, or the erase or program status. Status Register indicates the status of the partition, not WSM. Even if the status register bit SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.
The status register reports if an erase or program operation to each partition has been successfully completed, and if not, indicates a reason for the error. This register cannot be set, only can be cleared by writing the Clear Status Register command or by resetting the device.

2.4 Data Protection

Block lock bit and block lock-down bit can be set for each block, to protect the data within its block.

If the RST# is driven low (V_{IL}), or if the voltage on the V_{CC} pin is below the write lock out voltage (V_{LKO}), or if the voltage on the V_{PP} pin is below the write lock out voltage (V_{PPLK}), then all write functions including OTP program are disabled.

The system should be designed to switch the voltage on V_{PP} below the write lock out voltage (V_{PPLK}) for read cycles. This scheme provides the data protection at the hardware level. The two-cycle command sequence architecture for block erase, full chip erase, (page buffer) program, OTP program, and block lock configuration provides the data protection at the software level against data alternation.

3 Bus Operation

The system CPU reads and writes the flash memory. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. Table 4 lists the bus operation.

The function which is available varies according to each product. Refer to the specifications whether each function in this document is available or not. The function which is not described in the specifications can not be used for that product, even if that function is explained in this section.

3.1 Read Array

The product has five control pins (CE#, OE#, WE#, RST# and WP#). When RST# is V_{IH}, read operations access the memory array, status register, identifier codes, OTP block and query codes independent of the voltage on V_{PP}.

The device is automatically initialized upon power-up or device reset mode and set to asynchronous read mode in which 8-word page mode is available. As necessary, write the appropriate read command (Read Array, Read Identifier codes/OTP, Read Query or Read Status Register command) with the partition address to the CUI (Command User Interface). The CUI decodes the partition address and set the target partition to the appropriate read mode.

Asynchronous page mode is available only for main array, that is, parameter blocks and main blocks. Read operations for status register, identifier codes, OTP block and query codes support single asynchronous read cycle.

To read data from the product, RST# and WE# must be at V_{IH}, and CE# and OE# at V_{IL}. CE# is the device selection control, and CE#-low enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and OE#-low drives the selected memory data onto the I/O bus.

3.2 Output Disable

With OE# at V_{IH}, the device outputs are disabled. Output pins DQ_0 - DQ_{15} are placed in a high-impedance (High Z) state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the product in standby mode.

In standby mode, the product substantially reduces its power consumption because almost of all internal circuits are inactive. DQ_0-DQ_{15} outputs a High Z state independent of OE#. Even if CE# is set to V_{IH} during block erase, full chip erase, (page buffer) program or OTP program, the device continues the operation and consumes active power until the completion of the operation.

3.4 Reset

Driving RST# to logic-low level (V_{IL}) places the product in reset mode.

If RST# is held V_{IL} for a minimum t_{PLPH} in read modes, the device is deselected and internal circuitry is turned off. Outputs are placed in a High Z state. Status register is set to 80H. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The device returns to the initial mode described in Section 2.1.

During block erase, full chip erase, (page buffer) program or OTP program mode, RST#-low will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or programmed. Status register bit SR.7 remains "0" until the reset operation has been completed. After RST# goes to V_{IH}, time t_{PHWL} and t_{PHEL} is required before another command can be written.

As with any automated device, it is important to assert RST# during system reset. When the system comes out of reset, it expects to read the data from the flash memory. The product allows proper CPU initialization following a system reset through the use of the RST# input. In this application, RST# is controlled by the same RESET# signal that resets the system CPU. After return from reset mode, the product is automatically set to asynchronous read mode in which 8-word page mode is available. Delay time t_{PHQV} is required until memory access outputs are valid.

Table 4. Bus Operation[1, 2]

Mode	Notes	RST#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-15}	RY/BY# [8]
Read Array	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset	3	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Table 6 through Table 8	X	See Table 6 through Table 8	X
Read Query	6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Section 6	X	See Section 6	X
Write	4,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:
1. Refer to DC Characteristics. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when $V_{PP}=V_{PPH1/2}$ and V_{CC} is the specified voltage.
   Command writes involving full chip erase are reliably executed when $V_{PP}=V_{PPH1}$ and V_{CC} is the specified voltage.
5. Refer to Table 5 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Section 6 for more information about query code.
8. RY/BY# is V_{OL} when the WSM (Write State Machine) is executing internal block erase, full chip erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.

3.5 Read Identifier Codes/OTP

The manufacturer code, device code, block lock configuration codes, partition configuration register code and the data within the OTP block can be read in the read identifier codes/OTP mode (see Table 6 through Table 8). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

3.6 Read Query

CFI (Common Flash Interface) code, which is called query code, can be read after writing the Read Query command. The address to read query code should be in the partition address which is written with the Read Query command. The CFI data structure contains information such as block size, density, command set and electrical specifications (see Section 6). In this mode, read cycles retrieve CFI information. To return to read array mode, write the Read Array command (FFH) with the partition address.

3.7 Write the Command to the CUI

Except for the Full Chip Erase command, writing commands to the CUI always requires the word address, block address or partition address. Before writing the Block Erase command, Full Chip Erase command, (Page Buffer) Program command or OTP Program command, WSM (Write State Machine) should be ready and not be used in any partition.

Applying the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP} enables successful block erase, (page buffer) program or OTP program with writing the proper command and address to the CUI. Applying the specified voltage on V_{CC} and V_{PPH1} on V_{PP} enables successful full chip erase with writing the proper command to the CUI. Erase or program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

The Block Erase command requires appropriate command and an address within the block to be erased. The Full Chip Erase command requires appropriate command. The (Page Buffer) Program command requires appropriate command and an address of the location to be programmed. The Set/Clear Block Lock Bit or Set Block Lock-down Bit command requires appropriate command and an address within the target block. The OTP Program command requires appropriate command and an address of the location to be programmed within the OTP block. The Set Partition Configuration Register command requires appropriate command and configuration register code presented on the addresses A_0-A_{15}.

The CUI itself does not occupy an addressable memory location. When both CE# and WE# go V_{IL} (valid), the command is written to CUI and the address and data are latched on the rising edge of CE# or WE#, whichever goes high first. The command can be written to the CUI at the standard microprocessor writing timing.

4 Command Definitions

Operations of the device are selected by the specific commands written to the CUI (Command User Interface). Since commands are partition-specific, it is important to write commands within the target partition's address range (see Table 5).

The command which is available varies according to each product. Refer to the specifications whether each command in this document is available or not. The command which is not described in the specifications can not be used for that product, even if that command is explained in this section.

4.1 How to Write the Command

4.1.1 Using Dual Work Operation

The product supports dual work operation and the customer can store a flash memory interface software in the internal memory array of this device. To enable the flash memory interface software to be read at any time, the partition in which the flash memory interface software is stored must remain in the read array mode. Therefore, any command except for the Read Array command, the Full Chip Erase command (refer to Section 4.1.3) and the OTP Program command (refer to Section 4.1.3) must be written to the partition in which the flash memory interface software is not stored. For example, when the device is divided into two partitions such as partition 0, partition 1 and the flash memory interface software is stored in the partition 0, any command except for the commands mentioned above must be written to the partition 1. The following describes the reasons.

- All addresses which are written at the first cycle should be the same as the addresses which are written at the second cycle.
- All the commands except for the Full Chip Erase command and the OTP Program command require the partition address.

  Partition Address
  (Refer to Figure 2.1 through Figure 3.2 for the memory map)
  A_{20}-A_{16} (32M-bit device)
  A_{21}-A_{16} (64M-bit or 128M-bit device)

  When the command is written, the partition address must be placed on the address bus A_{20}-A_{16} or A_{21}-A_{16} at the first, second and subsequent command cycle.

- Each command except for the Full Chip Erase command and the OTP Program command affects only the mode of the partition to which the command is written.
- After the first cycle command of block erase (20H), program (40H or 10H), set/clear block lock bit (60H), set block lock-down bit (60H), or set partition configuration register (60H) is written, the target partition to which the command is written is put into the read status register mode. Subsequent read operations to that partition output the status register data of its partition.
- After the first cycle command of page buffer program (E8H) is written, the target partition to which the command is written is put into the read extended status register mode. Subsequent read operations to that partition output the extended status register data.
- After the second cycle command of block erase (D0H), program (data to be programmed), set block lock bit (01H), clear block lock bit (D0H) or set block lock-down bit (2FH) is written, the target partition to which the command is written remains in the read status register mode.
- After the second cycle command of set partition configuration register (04H) is written and the operation is successfully completed, all the partitions return to the read array mode. If the operation is not completed successfully, the target partition to which the command is written remains in the read status register mode.
- After the second and subsequent cycle commands of page buffer program are written, the target partition to which the command is written is put into the read status register mode. Subsequent read operations to that partition output the status register data of its partition.

4.1.2 Not Using Dual Work Operation

In this case, the flash memory interface software must be stored in the external ROM area. The command can be written to any partition. However, all first and second cycle command addresses should be the same and the commands require the partition address.

4.1.3 Full Chip Erase and OTP Program

Full chip erase and OTP program are different from other modes, in which dual work operation is not available. The following describes the reasons.

- After the first cycle command of full chip erase (30H) or OTP program (C0H) is written to any partition, all the partitions are put into the read status register mode. Subsequent read operations to any partition output the status register data. The memory array data cannot be read in these modes.
- After the second cycle command of full chip erase (D0H) or OTP program (data to be programmed) is written to any partition, all the partitions remain in the read status register mode. Subsequent read operations to any partition output the status register data. The memory array data cannot be read in these modes.

To read the memory array data, write the Read Array command (FFH) after the full chip erase or OTP program operation has been successfully completed.

When full chip erase or OTP program operation is used, the customer must store the flash memory interface software that initiates and polls progress of full chip erase or OTP program to the external ROM area.

4.2 Read Array Command

Upon initial device power-up or after reset mode, all the partitions in the device default to asynchronous read mode in which 8-word page mode is available. The Read Array command to a partition places the partition to read array mode. The partition remains enabled for read array mode until another valid command is written to the partition. When RST# is at V_{IH}, the Read Array command is valid independent of the voltage on V_{PP}. Once the internal WSM (Write State Machine) has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Array command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Array command can be accepted in other partitions except for full chip erase or OTP program operation.

Since the product provide dual work capability, partitions not executing block erase or (page buffer) program operation are allowed to set to the read array mode and the memory array data within the partitions can be read without suspending block erase or (page buffer) program operation.

4.3 Read Identifier Codes/OTP Command

The read identifier codes/OTP mode is initiated by writing the Read Identifier Codes/OTP command (90H) to the target partition. Read operations to that partition output the identifier codes or the data within the OTP block. To terminate the operation, write another valid command to the partition. In this mode, the manufacturer code, device code, block lock configuration codes, partition configuration register code and the data within the OTP block as well as the OTP block lock state can be read on the addresses shown in Table 6 through Table 8. Once the internal WSM has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Identifier Codes/OTP command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Identifier Codes/ OTP command can be accepted in other partitions except for full chip erase or OTP program operation. Like the Read Array command, the Read Identifier Codes/OTP command functions independently of the V_{PP} voltage and RST# must be at V_{IH}.

To read the data in the OTP block, it is important to write addresses within the OTP area's address range (refer to Table 6 through Table 8).

Asynchronous page mode is not available for reading identifier codes/OTP. Read operations for identifier codes or OTP block support single asynchronous read cycle.

Table 5. Command Definitions(11)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data	Oper(1)	Addr(2)	Data(3)
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5,9	Write	X	30H	Write	X	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	C0H	Write	OA	OD
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

NOTES:

1. Bus operations are defined in Table 4.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See Table 6 through Table 8).
   QA=Query codes address. Refer to Section 6 for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 4).
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes. (See Table 6 through Table 8).
   QD=Data read from query database. Refer to Section 6 for details.
   SRD=Data read from status register. See Table 9 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 6 through Table 8). The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Section 4.10 for

details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Identifier Codes and OTP Address for Read Operation (7)

	Code	Address [A_{15}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	1
Device Code	Top Parameter Device Code	0001H	Refer to specifications	1, 2
	Bottom Parameter Device Code	0001H		1, 2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ_0 = 0	3
	Block is Locked		DQ_0 = 1	3
	Block is not Locked-Down		DQ_1 = 0	3
	Block is Locked-Down		DQ_1 = 1	3
Device Configuration Code	Partition Configuration Register	0006H	PCRC	1, 4
OTP	OTP Lock	0080H	OTP-LK	1, 5
	OTP	0081-0088H	OTP	1, 6

NOTES:
1. The address A_{21}, A_{20}-A_{16} are shown in below table for reading the manufacturer code, device code, device configuration code and OTP data.
2. Top parameter device has its parameter blocks in the plane3 (The highest address). Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
3. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written. DQ_{15}-DQ_2 are reserved for future implementation.
4. PCRC=Partition Configuration Register Code.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.

7. Refer to the specifications for the information of the product which has two or more BE# (CE#) pins or which has 32-bit I/O interface.

Table 7. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1) (32M-bit device)

Partition Configuration Register (2)			Address (32M-bit device)
PCR.10	PCR.9	PCR.8	[A_{20}-A_{16}]
0	0	0	00H
0	0	1	00H or 08H
0	1	0	00H or 10H
1	0	0	00H or 18H
0	1	1	00H or 08H or 10H
1	1	0	00H or 10H or 18H
1	0	1	00H or 08H or 18H
1	1	1	00H or 08H or 10H or 18H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 14 for the partition configuration register.

Table 8. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1) (64M-bit device)

Partition Configuration Register (2)			Address (64M-bit device)
PCR.10	PCR.9	PCR.8	[A_{21}-A_{16}]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 14 for the partition configuration register.

4.4 Read Query Command

The read query mode is initiated by writing the Read Query command (98H) to the target partition. Read operations to that partition output the query code (Common Flash Interface code) shown in Section 6. To terminate the operation, write another valid command to the partition. Once the internal WSM has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Query command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Query command can be accepted in other partitions except for full chip erase or OTP program operation. Like the Read Array command, the Read Query command functions independently of the V_{PP} voltage and RST# must be at V_{IH}. Refer to Section 6 for more information about query code.

Asynchronous page mode is not available for reading query code. Read operations for query code support single asynchronous read cycle.

4.5 Read Status Register Command

The status register may be read to determine when block erase, full chip erase, (page buffer) program or OTP program has been completed and whether the operation has been successfully completed or not (see Table 9). The status register can be read at any time by writing the Read Status Register command (70H) to the target partition. Subsequent read operations to that partition output the status register data until another valid command is written. The status register contents are latched on the falling edge of OE# or CE# whichever occurs later. This requires address setup time (t_{AVGL} or t_{AVEL}) to and address hold time (t_{GLAX} or t_{ELAX}) from the later falling edge of OE# or CE#. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage and RST# must be at V_{IH}.

Asynchronous page mode is not available for reading status register. Read operations for status register support single asynchronous read cycle.

During the dual work operation, the status register data is read from the partition which is executing block erase or (page buffer) program operation. The memory array data can be read from other partitions which are not executing block erase or (page buffer) program operation. The partition to be accessed is automatically identified according to the input address.

4.6 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 that have been set to "1"s by the WSM can only be cleared by writing the Clear Status Register command (50H). This command functions independently of the V_{PP} voltage. RST# must be at V_{IH}. To clear the status register, write the Clear Status Register command and an address within the target partition to the CUI.

Status register bits SR.5, SR.4, SR.3 and SR.1 indicate various error conditions occurring after writing commands (see Table 9). When erasing multiple blocks or programming several words in sequence, clear these bits before starting each operation. The status register bits indicate an error for during the sequence.

After executing the Clear Status Register command, the partition returns to read array mode. This command clears only the status register of the addressed partition. During block erase suspend or (page buffer) program suspend, the Clear Status Register command is invalid and the status register cannot be cleared.

Table 9. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
- 1 = Ready
- 0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
- 1 = Error in (Page Buffer) Program or OTP Program
- 0 = Successful (Page Buffer) Program or OTP Program

SR.3 = V_{PP} STATUS (VPPS)
- 1 = V_{PP} LOW Detect, Operation Abort
- 0 = V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 or RY/BY# to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, V_{PPH2} or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 10. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
- 1 = Page Buffer Program available
- 0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:
After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

4.7 Block Erase Command

The two-cycle Block Erase command initiates one block erase at the addressed block within the target partition. Read operations to that partition output the status register data of its partition. At the first cycle, command (20H) and an address within the block to be erased is written to the CUI, and command (D0H) and the same address as the first cycle is written at the second cycle. Once the Block Erase command is successfully written, the WSM automatically starts erase and verification processes. The data in the selected block are erased (becomes FFFFH). The system CPU can detect the block erase completion by analyzing the output data of the status register bit SR.7. The partition including the block to be erased remains in read status register mode after the completion of the block erase operation until another command is written to the CUI. Figure 5.1 and Figure 5.2 show a flowchart of the block erase operation.

Check the status register bit SR.5 at the end of block erase. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The partition remains in read status register mode until a new command is written to that partition.

This two-cycle command sequence ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in status register bits SR.5 and SR.4 of the partition being set to "1" and the operation will be aborted.

For reliable block erase operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, block erase operations are not guaranteed. For example, attempting a block erase at $V_{PP} \leq V_{PPLK}$ causes SR.5 and SR.3 being set to "1". Also, successful block erase requires that the selected block is unlocked. When block erase is attempted to the locked block, bits SR.5 and SR.1 will be set to "1".

Block erase operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

4.8 Full Chip Erase Command

The two-cycle Full Chip Erase command erases all of the unlocked blocks. Before writing this command, all of the partitions should be ready (WSM should not be occupied by any partition). At the first cycle, command (30H) is written to the CUI, and command (D0H) is written at the second cycle. After writing the command, the device outputs the status register data when any address within the device is selected. The WSM automatically starts the erase operation for all unlocked blocks, skipping the locked blocks. The full chip erase operation cannot be suspended through the erase suspend command (described later). The system CPU can detect the full chip erase completion by analyzing the output data of the status register bit SR.7. All the partitions remain in the read status register mode after the completion of the full chip erase operation until another command is written to the CUI. Figure 6.1 and Figure 6.2 show a flowchart of the full chip erase operation.

The WSM aborts the operation upon encountering an error during the full chip erase operation and leaves the remaining blocks not erased. After the full chip erase operation, check the status register bit SR.5. When a full chip erase error is detected, SR5 of all partitions will be set to "1". The status registers for all partitions should be cleared before system software attempts corrective actions. After that, retry the Full Chip Erase command or erase block by block using the Block Erase command.

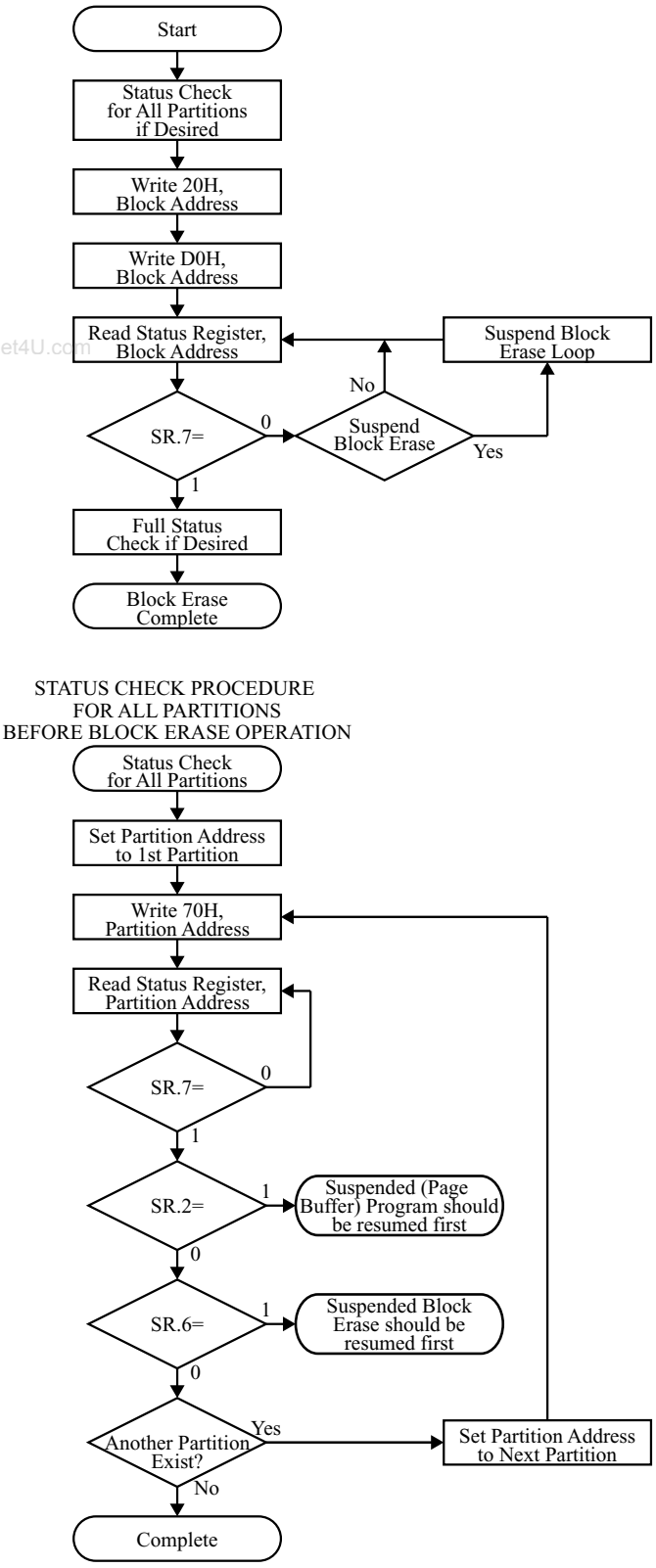
This two-cycle command sequence ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in status register bits SR.5 and SR.4 of all partitions being set to "1" and the operation will be aborted.

For reliable full chip erase operation, apply the specified voltage on V_{CC} and V_{PPH1} on V_{PP}. In the absence of this voltage, full chip erase operations are not guaranteed. For example, attempting a full chip erase at $V_{PP} \leq V_{PPLK}$ causes SR.5 and SR.3 being set to "1". The full chip erase operation with applying V_{PPH2} on V_{PP} is inhibited for some products. Refer to the specifications whether the full chip erase operation with applying V_{PPH2} on V_{PP} is available or not.

As previously mentioned, the Full Chip Erase command erases all blocks except for the locked blocks. Unlike the block erase, the status register bits SR.5 and SR.1 are not set to "1" even if the locked block is included. However, when all blocks are locked, the bits SR.5 and SR.1 are set to "1" and the operation will not be executed.

If an error is detected during the full chip erase operation, error bits for status registers in all partitions are set to "1". This requires that the Clear Status Register command be written to all partitions to clear the error bits.

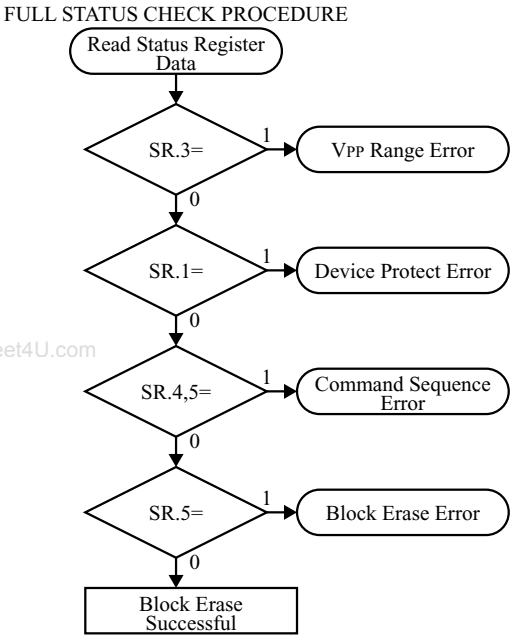
Dual work operation is not available during the full chip erase mode. The memory array data cannot be read in this mode. To return to the read array mode, write the Read Array command (FFH) to the CUI after the completion of the full chip erase operation.



Bus Operation	Command	Comments
Write	Block Erase	<First cycle> Data=20H Addr=Within Block to be Erased
		<Second cycle> Data=D0H Addr=Within Block to be Erased
Read		Status Register Data Addr=Within Block to be Erased
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
When subsequently erasing a block, repeat the above sequence. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after a sequence of block erasures to place device in read array mode.		

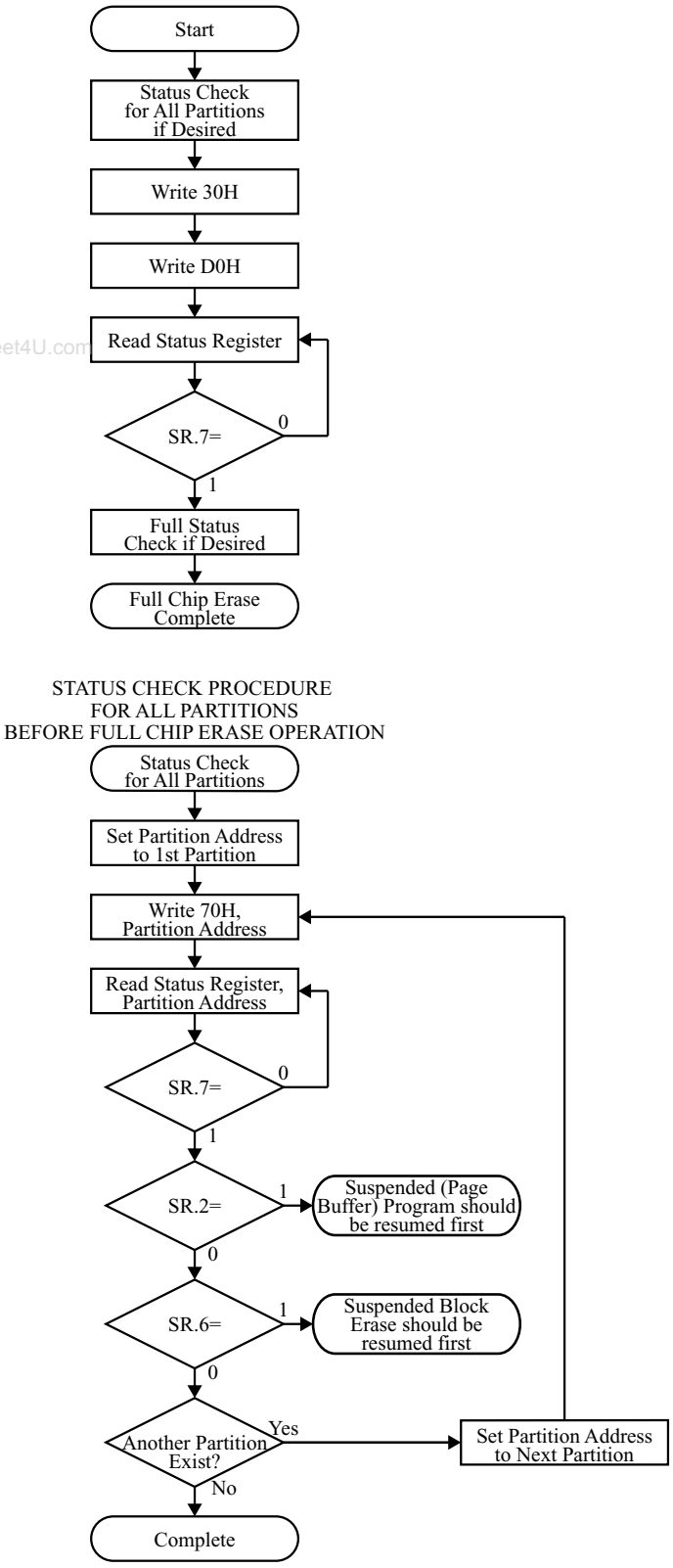
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed

Figure 5.1. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

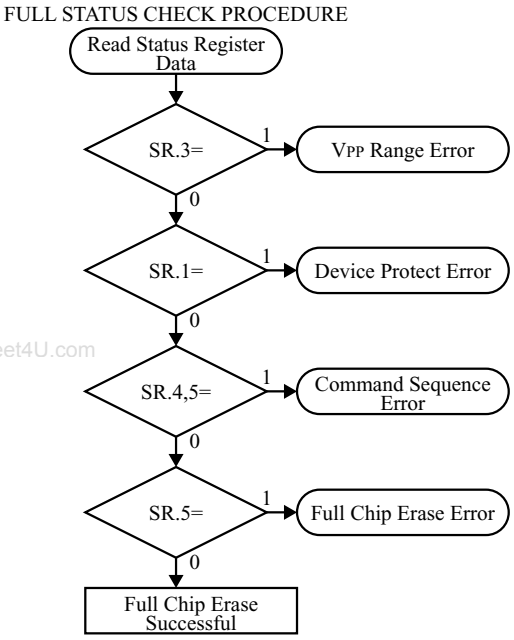
Figure 5.2. Automated Block Erase Flowchart (Continued)



Bus Operation	Command	Comments
Write	Full Chip Erase	<First cycle> Data=30H Addr=X
		<Second cycle> Data=D0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Check the status after full chip erase. Write FFH after the full chip erase to place device in read array mode.		

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed

Figure 6.1. Automated Full Chip Erase Flowchart



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect All Blocks are locked.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 6.2. Automated Full Chip Erase Flowchart (Continued)

4.9 Program Command

A two-cycle command sequence written to the target partition initiates a word program operation. Read operations to the target partition to be programmed output the status register data until another valid command is written. At the first cycle, write command (standard 40H or alternate 10H) and an address of memory location to be programmed, followed by the second write that specifies the address and data. The WSM then takes over, controlling the internal word program algorithm. The system CPU can detect the word program completion by analyzing the output data of the status register bit SR.7. Figure 8.1 and Figure 8.2 show a program flowchart.

The internal WSM verify only detects errors for "1"s that are not successfully programmed to "0"s. Check the status register bit SR.4 at the end of word program. If a word program error is detected, the status register should be cleared before system software attempts corrective actions. The partition remains in read status register mode until it receives another command.

For reliable word program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, word program operations are not guaranteed. For example, attempting a word program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". Also, successful word program requires for the selected block is unlocked. When word program is attempted to the locked block, bits SR.4 and SR.1 will be set to "1".

Word program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

4.10 Page Buffer Program Command

The product has 16-word page buffer, which can perform fast sequential programming up to 16 words. However, this 16-word address must be inside every 4K-word address range XXX000H-XXXFFFH, as shown in Figure 7. When programming across this 4K-word address range, sequence error occurs and status register bits SR.5 and SR.4 are set to "1". The data are once loaded to the page buffer and programmed to the flash array when the confirm command (D0H) is written. See the flowchart in Figure 9.1 and Figure 9.2.

The page buffer program is executed by at least four-cycle or up to 19-cycle command sequence. First, write the Page Buffer Program setup command (E8H) and start address to the partition's CUI. At this point, read operations to the target partition to be programmed output the extended status register data (see Table 10). Check the extended status register data. When XSR.7 is set to "1", the setup command written is valid. Then, at the second cycle, write the word count [N]-1 and start address if the number of words to be programmed is [N] in total. That is, when the number of [N] is 1 word, write (00H); if [N] is 16 words, write (0FH). The word count [N]-1 must be less than or equal to 0FH. Attempting to write more than 0FH for the word count causes the sequence error and the status register bits SR.5 and SR.4 are set to "1". After writing a word count [N]-1, read operations to the target partition to be programmed output the status register data. At the third cycle following the write of [N]-1, write the first data to be programmed and start address to the partition's CUI. Lower 4 bits (A_0-A_3) of the start address also correspond to the page buffer address and the data are stored in the page buffer. At the fourth and subsequent cycles, write additional data and address, depending on the count. All subsequent address must lie within the start address plus the count. After writing the Nth word data, write the confirm command (D0H) and an address within the target block to be programmed at the last cycle. This initiates the WSM to being transferring the data from the page buffer to the flash array. If a command other than the confirm command (D0H) is written, sequence error occurs and status register bits SR.5 and SR.4 of the partition are set to "1". When the data are transferred from the page buffer to the flash array, the status register bit SR.7 is set to "0". Then, the target partition is in the page buffer program busy mode.

If the Page Buffer Program command is attempted past an erase block boundary, the device will program the data to the flash array up to an erase block boundary and then stop programming. The status register bits SR.5 and SR.4 will be set to "1" (command sequence error). SR.5 and SR.4 should be cleared before writing next command.

For reliable page buffer program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, page buffer program operations are not guaranteed. For example, attempting a page buffer program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". Also, successful page buffer program requires for the selected block is unlocked. When page buffer program is attempted to the locked block, bits SR.4 and SR.1 will be set to "1".

During page buffer program, dual work operation is available. The array data can be read from partitions not being programmed.

Page buffer program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

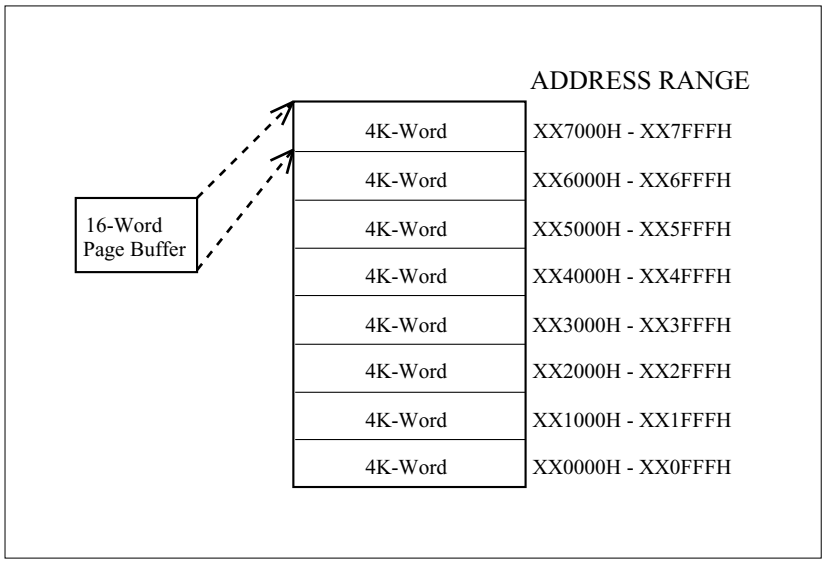
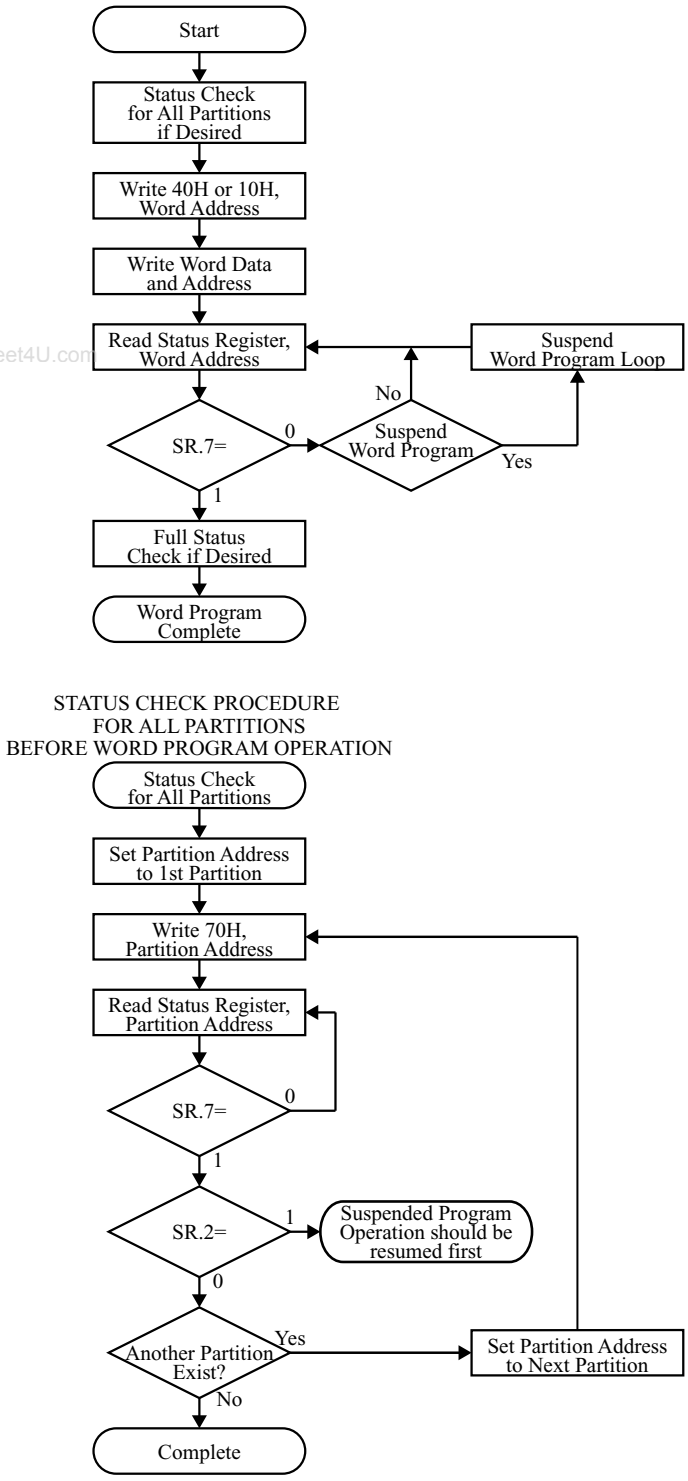


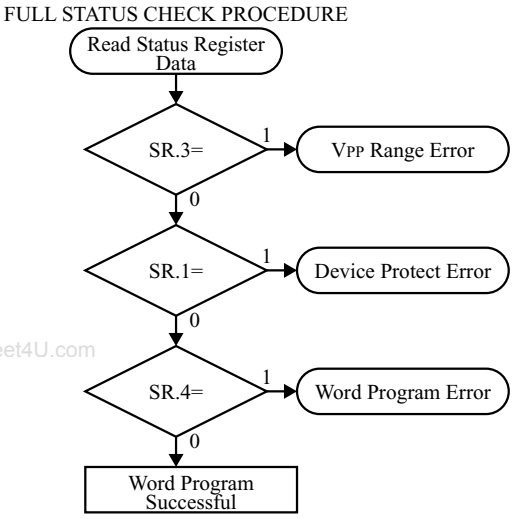
Figure 7. 32K-Word Block



Bus Operation	Command	Comments
Write	Word Program	<First cycle> Data=40H or 10H Addr=Location to be Programmed
		<Second cycle> Data= Data to be Programmed Addr=Location to be Programmed
Read		Status Register Data Addr=Location to be Programmed
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat the above sequence for the subsequent word programs. SR full status check can be done after each word program, or after a sequence of word programs. Write FFH after a sequence of word programs to place device in read array mode.		

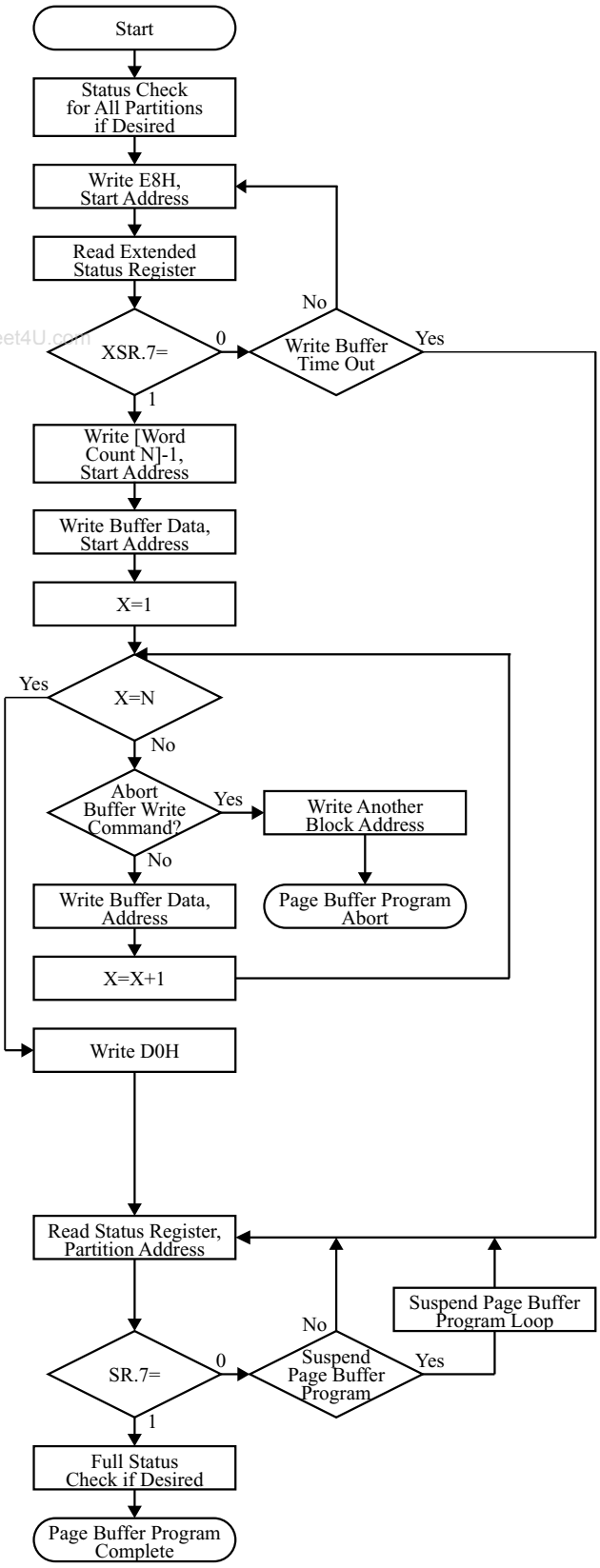
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Program Suspended 0=Program Completed

Figure 8.1. Automated Program Flowchart



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4 1=Word Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 8.2. Automated Program Flowchart (Continued)

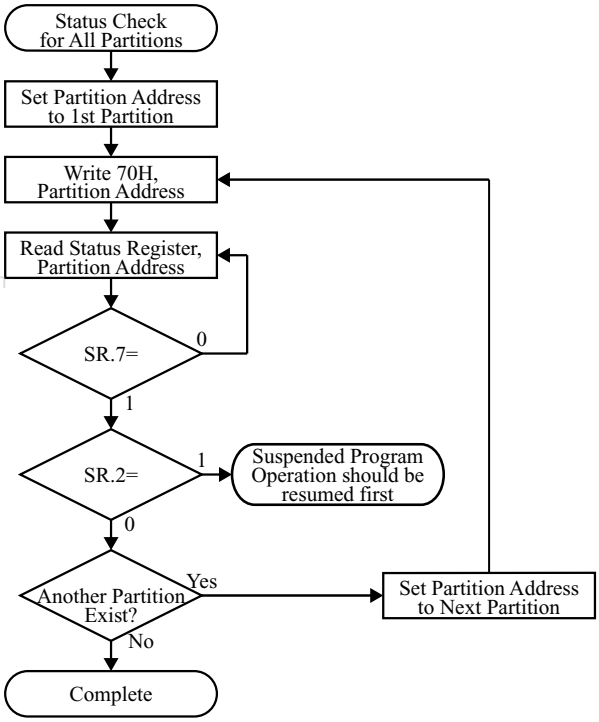


Bus Operation	Command	Comments
Write	Page Buffer Program	<First cycle> Data=E8H Addr=Start Address
Read		Extended Status Register Data
Standby		Check XSR.7 1=Page Buffer Program Ready 0=Page Buffer Program Busy
Write (Note 1)	Page Buffer Program	<Second cycle> Data=[Word Count N]-1 Addr=Start Address
Write (Note 2, 3)		<Third cycle> Data=Buffer Data Addr=Start Address
Write (Note 4, 5)		<(N+2)th cycle> Data=Buffer Data Addr=Sequential Address following start address
Write		<(N+3)th cycle> Data=D0H Addr=Within Block
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

1. Word count values on DQ_{0-7} are loaded into count register.
2. Write Buffer contents will be programmed at the start address.
3. Align the start address on a Write Buffer boundary for maximum programming performance.
4. The device aborts the Page Buffer Program command if the current address is outside of the original block address.
5. The Status Register indicates an “improper command sequence” if the Page Buffer Program command is aborted. Follow this with a Clear Status Register command.
   SR full status check can be done after each page buffer program, or after a sequence of page buffer programs.
   Write FFH after the last page buffer program operation to place device in read array mode.

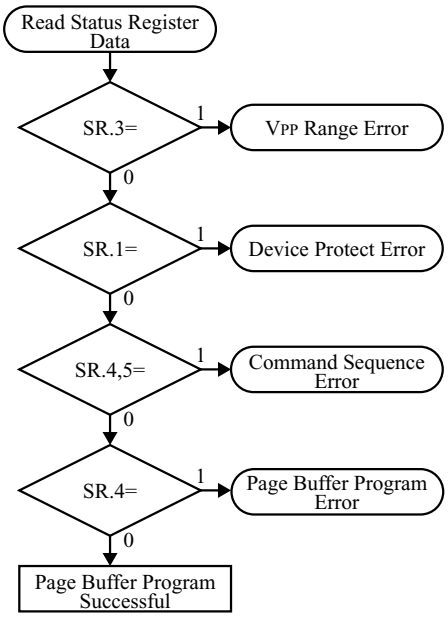
Figure 9.1. Automated Page Buffer Program Flowchart

STATUS CHECK PROCEDURE
FOR ALL PARTITIONS BEFORE
PAGE BUFFER PROGRAM OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Program Suspended 0=Program Completed

FULL STATUS CHECK PROCEDURE FOR
PAGE BUFFER PROGRAM OPERATION



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Page Buffer Program Error
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 9.2. Automated Page Buffer Program Flowchart (Continued)

4.11 Block Erase Suspend Command and Block Erase Resume Command

The Block Erase Suspend command (B0H) allows block erase interruption to read or program data in the blocks other than that which is suspended. This command is valid for the block erase operation and the full chip erase operation can not be suspended.

Once the block erase process starts in a partition, writing the Block Erase Suspend command to the partition requests that the WSM suspends the block erase sequence at a predetermined point in the algorithm. Read operations to the target partition after writing the Block Erase Suspend command access the status register. Status register bits SR.7 and SR.6 indicate if the block erase operation has been suspended (both will be set to "1"). Specification t_{WHRH2} or t_{EHRH2} defines the block erase suspend latency.

When the Block Erase Suspend command is written after the completion of the block erase operation, the partition returns to read array mode. Therefore, the Read Status Register command (70H) must be written to the target partition after writing the Block Erase Suspend command. If the status register bits SR.7 and SR.6 are set to "1", block erase has been suspended.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Page Buffer) Program command sequence can also be written during block erase suspend to program data in other blocks. Using the (Page Buffer) Program Suspend command (see Section 4.12), a program operation can also be suspended during a block erase suspend.

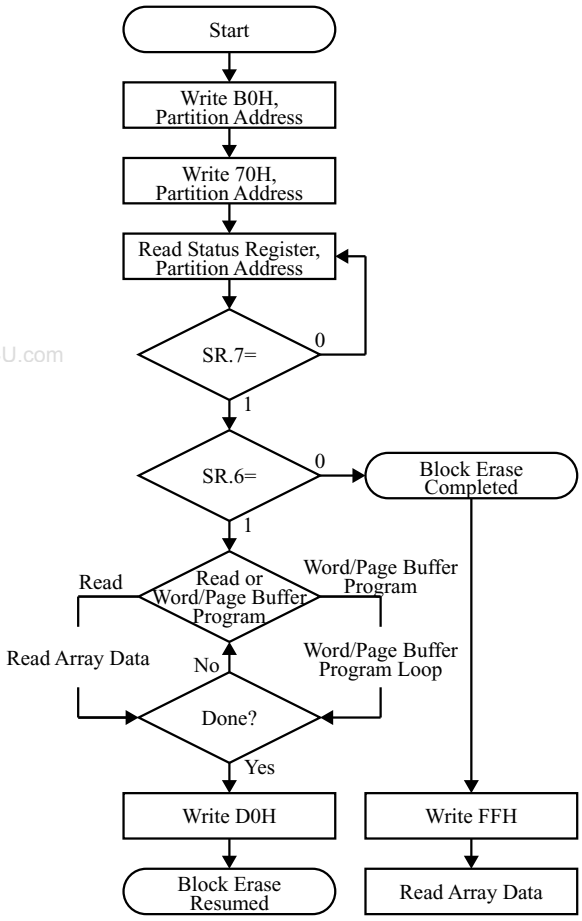
During a word program operation with block erase suspended, status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate the block erase suspend status.

If the Page Buffer Program setup command (E8H) is written to the target partition during block erase suspend in which SR.7 and SR.6 are set to "1", read operations to the target partition to be programmed output the extended status register data. In read extended status register mode, bit XSR.7 is only valid, which indicates that the written command (E8H) is available, and other bits (from XSR.6 to XSR.0) are invalid (see Table 10). When writing the word count [N]-1 and start address at next command cycle, the target partition returns to read status register mode and the status register bits SR.7 and SR.6 are set to "1". After the Page Buffer Program confirm command (D0H) is written, the status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate the block erase suspend status.

The valid commands while block erase is suspended are Read Array, Read Identifier Codes/OTP, Read Query, Read Status Register, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bit, Set Block Lock-down Bit and Block Erase Resume command. The commands other than those mentioned above are not accepted and should not be used during a block erase suspend.

To resume the block erase operation, write the Block Erase Resume command (D0H) to the partition. Status Register bits SR.7 and SR.6 will be automatically cleared. After the Block Erase Resume command is written, the target partition automatically outputs the status register data when read. V_{PP} must remain at $V_{PPH1/2}$ (at the same level before block erase suspended) while block erase is suspended. RST# must remain at V_{IH} and WP# must also remain at V_{IL} or V_{IH} (at the same level before block erase suspended). Block erase cannot resume until (page buffer) program operation initiated during block erase suspend is completed. Figure 10 shows the block erase suspend and block erase resume flowchart.

If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.



Bus Operation	Command	Comments
Write	Block Erase Suspend	Data=B0H Addr=Within Partition
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Block Erase Resume	Data=D0H Addr=Within Block to be Suspended

Figure 10. Block Erase Suspend and Block Erase Resume Flowchart

4.12 (Page Buffer) Program Suspend Command and (Page Buffer) Program Resume Command

The (Page Buffer) Program Suspend command (B0H) allows word and page buffer program interruption to read data from locations other than that which is suspended.

Once the (page buffer) program process starts in a partition, writing the (Page Buffer) Program Suspend command to the partition requests that the WSM suspends the (page buffer) program sequence at a predetermined point in the algorithm. Read operations to the target partition after writing the (Page Buffer) Program Suspend command access the status register. Status register bits SR.7 and SR.2 indicate if the (page buffer) program operation has been suspended (both will be set to "1"). Specification t_{WHRH1} or t_{EHRH1} defines the (page buffer) program suspend latency.

When the (Page Buffer) Program Suspend command is written after the completion of the (page buffer) program operation, the partition returns to read array mode. Therefore, the Read Status Register command (70H) must be written to the target partition after writing the (Page Buffer) Program Suspend command. If the status register bits SR.7 and SR.2 are set to "1", (page buffer) program has been suspended.

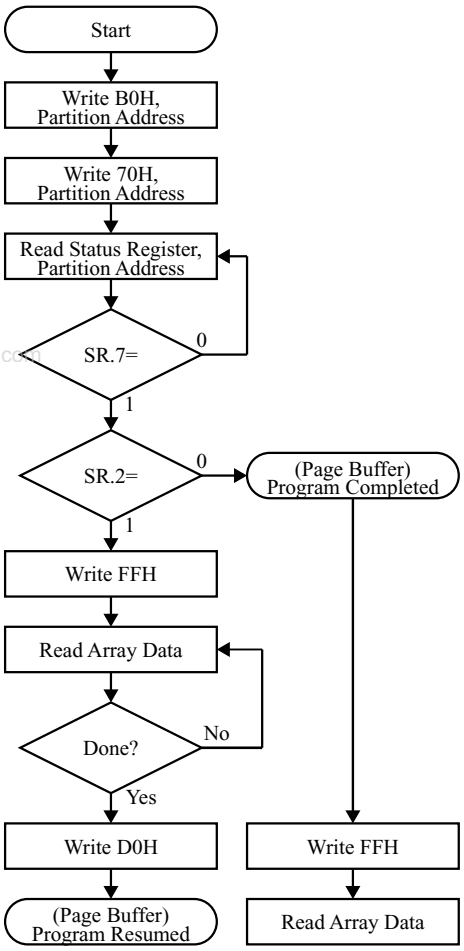
At this point, a Read Array command can be written to read data from locations other than that which is suspended.

The valid commands while (page buffer) program is suspended are Read Array, Read Identifier Codes/OTP, Read Query, Read Status Register and (Page Buffer) Program Resume command. The commands other than those mentioned above are not accepted and should not be used. For example, the block erase operation cannot be executed during a (page buffer) program suspend.

To resume the (page buffer) program operation, write the (Page Buffer) Program Resume command (D0H) to the partition. Status Register bits SR.7 and SR.2 will be automatically cleared. After the (Page Buffer) Program Resume command is written, the target partition automatically outputs the status register data when read. V_{PP} must remain at $V_{PPH1/2}$ (at the same level before (page buffer) program suspended) while (page buffer) program is suspended. RST# must remain at V_{IH} and WP# must also remain at V_{IL} or V_{IH} (at the same level before (page buffer) program suspended). Figure 11 shows the (page buffer) program suspend and (page buffer) program resume flowchart.

If the interval time from a (Page Buffer) Program Resume command to a subsequent (Page Buffer) Program Suspend command is short and its sequence is repeated, the (page buffer) program operation may not be finished.

After the (Page Buffer) Program Suspend command is written to the 1st partition to suspend the program operation while the 2nd partition is in block erase suspend mode, the (Page Buffer) Program Resume command should be written to the 1st partition first to resume the suspended (page buffer) program operation. After that, the Block Erase Resume command is written to the 2nd partition to resume the suspended block erase operation. If the Block Erase Resume command is written before the (Page Buffer) Program Resume command, the Block Erase Resume command is ignored and the partition to which the Block Erase Resume command is written is set to read array mode with block erase suspended.



Bus Operation	Command	Comments
Write	(Page Buffer) Program Suspend	Data=B0H Addr=Within Partition
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed
Write		Data=FFH Addr=Within Partition
Read		Read array locations from block other than that being programmed
Write	(Page Buffer) Program Resume	Data=D0H Addr=Location to be Suspended

Figure 11. (Page Buffer) Program Suspend and (Page Buffer) Program Resume Flowchart

4.13 Set Block Lock Bit Command

The product is provided with a block lock bit for each parameter block and main block. The features of set block lock bit is as follows:

- Any block can be independently locked by setting its block lock bit.
- The time required for block locking is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Block erase, full chip erase or (page buffer) program on a locked block cannot be executed (see Table 11 and Table 12).
- At power-up or device reset, all blocks default to locked state, regardless of the states before power-off or reset operation.
  (Lock bit is volatile.)

The Set Block Lock Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be locked is written to the target partition. At the second cycle, command (01H) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock bit is set within the minimum command cycle time and the corresponding block is locked. To check the lock status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock/unlock status is represented by the output pin DQ_0. If the output of DQ_0 is "1", the block lock bit is set correctly. Figure 12 shows set block lock bit flowchart.

The two-cycle command sequence ensures that block is not accidentally locked. An invalid Set Block Lock Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

The Set Block Lock Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

At power-up or device reset, since all blocks default to locked state, write the Clear Block Lock Bit command described later to clear block lock bit before a erase or program operation.

Table 11. Functions of Block Lock(5) and Block Lock-Down

Current State					Erase/Program Allowed (2)
State	WP#	DQ_1 (1)	DQ_0 (1)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](3)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](3)	1	0	1	Locked	No
[110](4)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

NOTES:
1. DQ_0=1: a block is locked; DQ_0=0: a block is unlocked.
   DQ_1=1: a block is locked-down; DQ_1=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
4. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 12. Block Locking State Transitions upon Command Write(4)

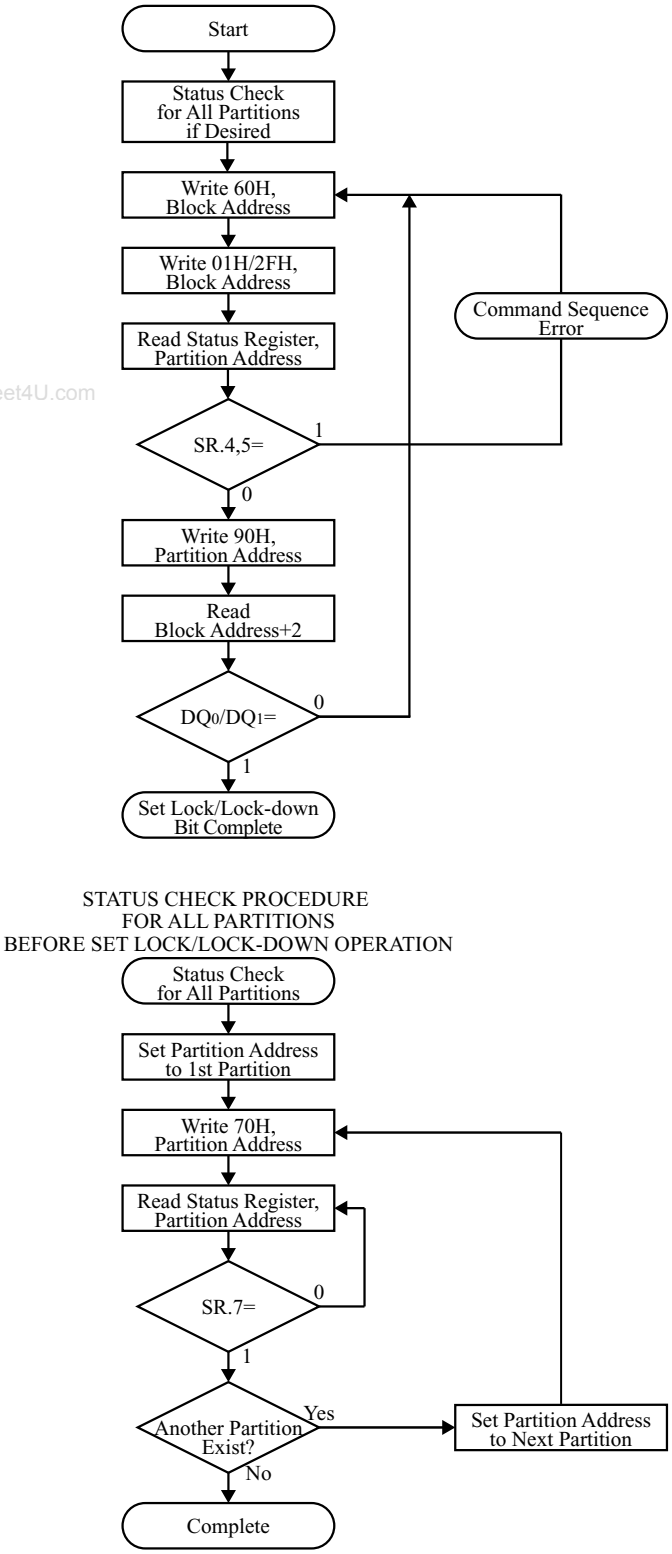
Current State				Result after Lock Command Written (Next State)		
State	WP#	DQ_1	DQ_0	Set Lock(1)	Clear Lock(1)	Set Lock-down(1)
[000]	0	0	0	[001]	No Change	[011](2)
[001]	0	0	1	No Change(3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111](2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111](2)
[111]	1	1	1	No Change	[110]	No Change

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH}.

Table 13. Block Locking State Transitions upon WP# Transition(4)

Previous State	Current State				Result after WP# Transition (Next State)	
	State	WP#	DQ_1	DQ_0	WP#=0→1(1)	WP#=1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

NOTES:
1. "WP#=0→1" means that WP# is driven to V_{IH} and "WP#=1→0" means that WP# is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.



Bus Operation	Command	Comments
Write	Set Block Lock Bit/Set Block Lock-down Bit	<First cycle> Data=60H Addr=Within Block to be Locked or Locked-down
		<Second cycle> Data= 01H (Lock Bit), or 2FH(Lock-down Bit) Addr=Within Block to be Locked or Locked-down
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Lock Bit or Lock-down Bit Data Addr=Block Address+2 (see Table 6 through Table 8)
Standby		Check DQ_0/DQ_1 1=Lock Bit or Lock-down Bit is Set
Repeat for the subsequent set block lock/lock-down bit. Lock status check can be done after each set block lock/lock-down bit operation or after a sequence of set block lock/lock-down bit operations. SR.5 and SR.4 are only cleared by the Clear Status Register command in cases where multiple block lock/lock-down bits are set before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery. Write FFH after a sequence of set block lock/lock-down bit operations to place device in read array mode.		

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 12. Set Block Lock Bit and Set Block Lock-down Bit Flowchart

4.14 Clear Block Lock Bit Command

A locked block can be unlocked by writing the Clear Block Lock Bit command. The features of clear block lock bit is as follows:

- Any block can be independently unlocked by clearing its block lock bit.
- The time required to be unlocked is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Block erase, full chip erase or (page buffer) program on an unlocked block can be executed (see Table 11 and Table 12).

The Clear Block Lock Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be unlocked is written to the target partition. At the second cycle, command (D0H) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock bit is cleared within the minimum command cycle time and the corresponding block is unlocked. To check the unlock status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock/unlock status is represented by the output pin DQ_0. If the output of DQ_0 is "0", the block lock bit is cleared correctly. Figure 13 shows clear block lock bit flowchart.

The two-cycle command sequence ensures that block is not accidentally unlocked. An invalid Clear Block Lock Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

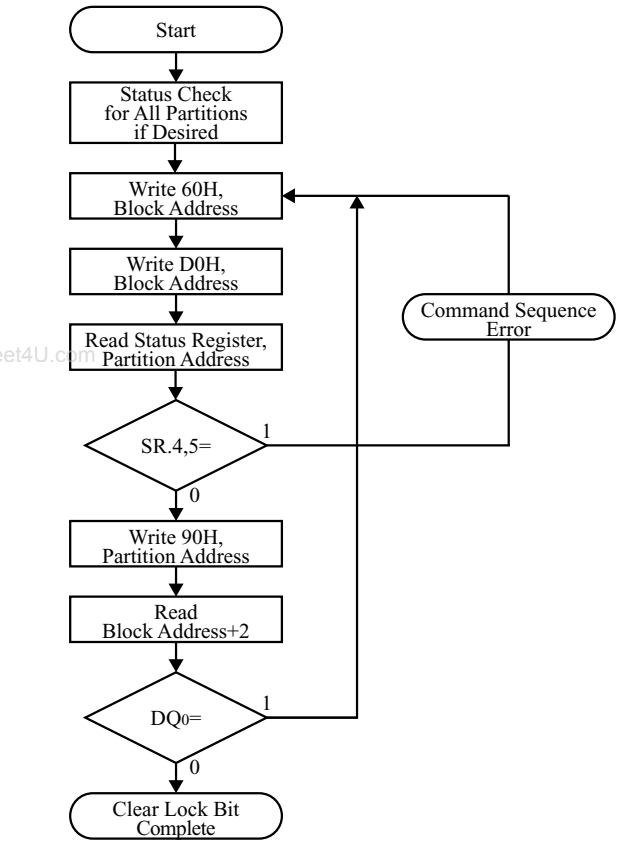
The Clear Block Lock Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

4.15 Set Block Lock-Down Bit Command

The block lock-down bit, when set, increases the security for data protection. The block lock-down bit has the following functions.

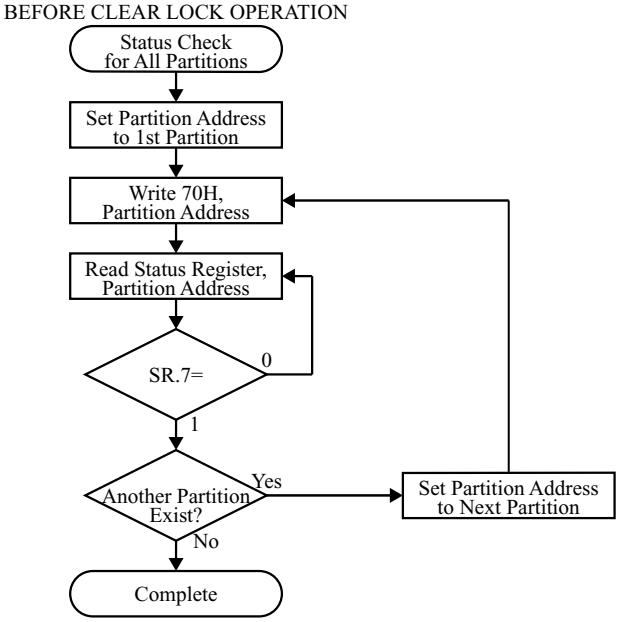
- Any block can be independently locked-down by setting its block lock-down bit.
- The time required to be locked-down is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Locked-down block is automatically locked regardless of WP# at V_{IL} or V_{IH}.
- When WP# is V_{IL}, locked-down blocks are protected from lock status changes.
- When WP# is V_{IH}, the lock-down bits are disabled and locked-down blocks can be individually unlocked by software command. These blocks can then be re-locked and unlocked as desired while WP# remains V_{IH}. When WP# goes V_{IL}, blocks that were previously marked lock-down return to the locked and locked-down state regardless of any changes made while WP# was V_{IH} (see Table 13).
- At power-up or device reset, all blocks are not locked-down regardless of the states before power-off or reset operation.
  (Lock-down bit is volatile.)
- Lock-down bit cannot be cleared by software, only by power-off or device reset.

The Set Block Lock-down Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be locked-down is written to the target partition. At the second cycle, command (2FH) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock-down bit is set within the minimum command cycle time and the corresponding block is locked-down. To check the lock-down status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock-down status is represented by the output pin DQ_1. If the output of DQ_1 is "1", the block lock-down bit is set correctly. Figure 12 shows set block lock-down bit flowchart.



Bus Operation	Command	Comments
Write	Clear Block Lock Bit	<First cycle> Data=60H Addr=Within Block to be Unlocked
		<Second cycle> Data= D0H Addr=Within Block to be Unlocked
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Lock Bit Data Addr=Block Address+2 (see Table 6 through Table 8)
Standby		Check DQ_0 0=Lock Bit is Cleared
Repeat for the subsequent clear block lock bit. Lock status check can be done after each clear block lock bit operation or after a sequence of clear block lock bit operations. SR.5 and SR.4 are only cleared by the Clear Status Register command in cases where multiple block lock bits are cleared before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery. Write FFH after a sequence of clear block lock bit operations to place device in read array mode.		

STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE CLEAR LOCK OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 13. Clear Block Lock Bit Flowchart

The two-cycle command sequence ensures that block is not accidentally locked-down. An invalid Set Block Lock-down Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

The Set Block Lock-down Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

At power-up or device reset, since no blocks are locked-down, write the Set Block Lock-down Bit command as necessary.

While WP# is V_{IH}, the lock-down bits are disabled but not cleared. Once any block is locked-down, it cannot be cleared until power-off or device reset.

4.16 OTP Program Command

OTP program is executed by a two-cycle command sequence. At the first cycle, command (C0H) and an address within the OTP block (see Figure 4) is written, followed by the second write that specifies the address and data. After writing the command, the device outputs the status register data when any address within the device is selected. The WSM then takes over, controlling the internal OTP program algorithm. The system CPU can detect the OTP program completion by analyzing the output data of the status register bit SR.7. Figure 14.1 and Figure 14.2 show OTP program flowchart.

The address written at the command cycle must be the address within the OTP block (refer to Figure 4). Writing an address outside the OTP block will cause a OTP program error and the status register bit SR.4 is set to "1". Clear the status register before writing next command.

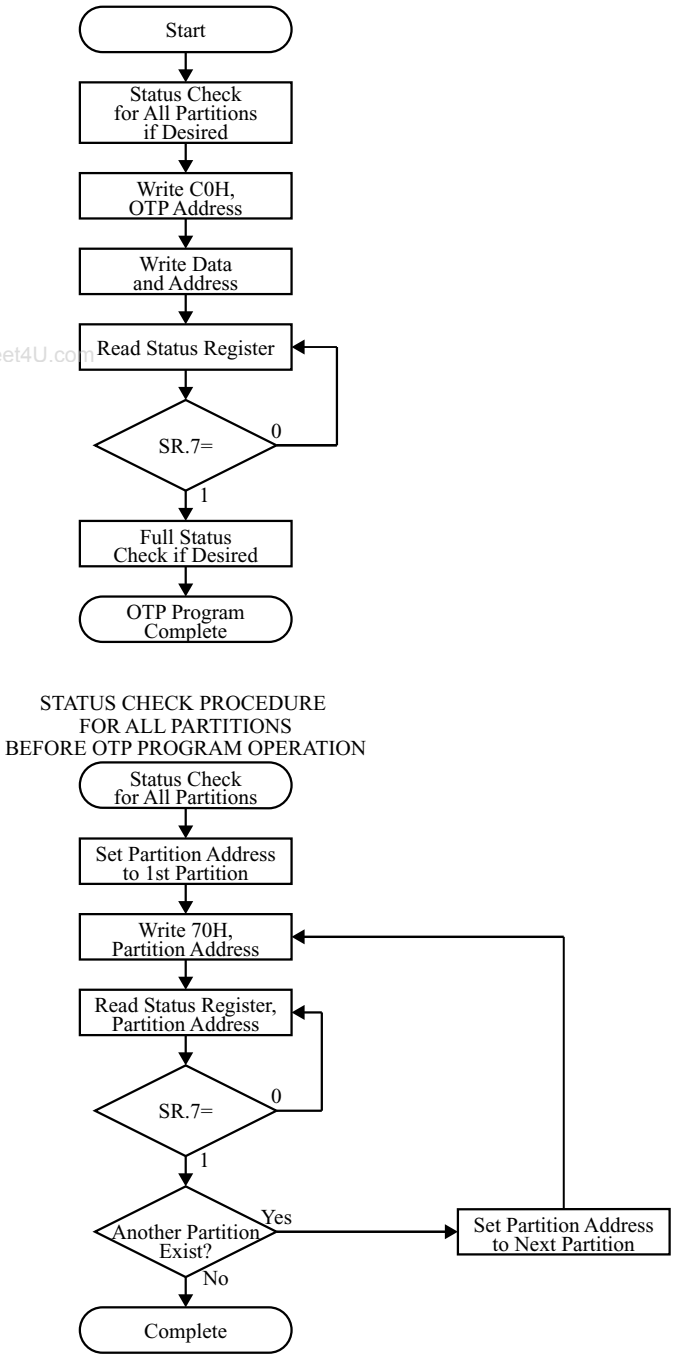
The internal WSM verify only detects errors for "1"s that are not successfully programmed to "0"s. Check the status register bit SR.4 at the end of OTP program. If a OTP program error is detected, the status register should be cleared before system software attempts corrective actions.

For reliable OTP program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, OTP program operations are not guaranteed. For example, attempting an OTP program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". OTP program operation on locked area causes SR.4 and SR.1 being set to "1" and the operation will not be executed.

OTP program cannot be suspended through the (Page Buffer) Program Suspend command (B0H). Even if the (Page Buffer) Program Suspend command is written during OTP program operation, the suspend command will be ignored.

If an error is detected during the OTP program operation, error bits for status registers in all partitions are set to "1". This requires that the Clear Status Register command be written to all partitions to clear the error bits.

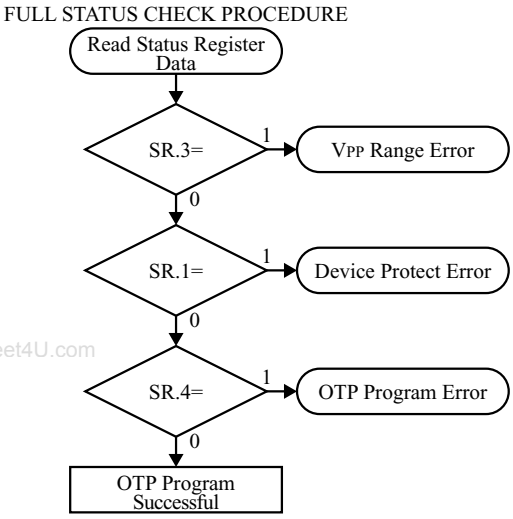
Dual work operation is not available while the OTP program mode, and the memory array data cannot be read even if that operation has been completed. To return to the read array mode, write the Read Array command (FFH) to the partition’s CUI after the completion of the OTP program operation.



Bus Operation	Command	Comments
Write	OTP Program	<First cycle> Data=C0H Addr=Location to be Programmed
Write		<Second cycle> Data=Data to be Programmed Addr=Location to be Programmed
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent OTP program. SR full status check can be done after each OTP program, or after a sequence of OTP programs. Write FFH after the OTP program operation to place device in read array mode.		

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 14.1. Automated OTP Program Flowchart



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=OTP Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 14.2. Automated OTP Program Flowchart (Continued)

4.17 Set Partition Configuration Register Command

The Partition Configuration Register (PCR) bits are set by writing the Set Partition Configuration Register command to the device.

This operation is initiated by a two-cycle command sequence. The partition configuration register can be configured by writing the command with the partition configuration register code. At the first cycle, command (60H) and a partition configuration register code is written. At the second cycle, command (04H) and the same address as the first cycle is written. The partition configuration register code is placed on the address bus, A_{15} - A_0, and is latched on the rising edge of CE#, or WE# (whichever occurs first). The partition configuration register code sets the partition boundaries. This command functions independently of the V_{PP} voltage. RST# must be at V_{IH}. After executing this command, the device returns to read array mode and status registers are cleared. Figure 16 shows set partition configuration register flowchart.

NOTES:
- The partition configuration register code can be read via the Read Identifier Codes/OTP command (90H). Address 0006H on A_{15} - A_0 contains the partition configuration register code (see Table 6 through Table 8).
- Partition configuration after device power-up or reset is as follows.
  (Partition configuration register bits are volatile.)
  Plane 0-2 are merged into one partition.
  (top parameter device)
  Plane1-3 are merged into one partition.
  (bottom parameter device)

4.17.1 How to Set the Partition Configuration Register

The partition configuration register is set by writing the Set Partition Configuration Register command, as previously described. The following summarizes how to set the partition configuration register.

- At the first cycle of the Set Partition Configuration Register command, write the following data and address.

  Data (Command)
  DQ_{15}-DQ_8=Any data.
  These bits do not affect the operation.
  DQ_7-DQ_0=60H

  Address
  A_{20}-A_{16}=Partition address (32M-bit device).
  A_{21}-A_{16}=Partition address (64M-bit or 128M-bit device).
  The partition address must be the address within the partition in which the flash memory interface software is not stored.
  A_{15}-A_{11}=Any address.
  These bits do not affect the operation.
  A_{10}-A_8=Partition configuration register code.
  These bits determine the partiton boundaries shown in Table 14 and Figure 15.
  A_7-A_0=Any address.
  These bits do not affect the operation.
- After writing the first cycle command (60H), the target partition to which the command is written is put into the read status register mode. Subsequent read operations to that partition output the status register data of its partition.
- At the second cycle of the Set Partition Configuration Register command, write the following data and address.

  Data (Command)
  DQ_{15}-DQ_8=Any data.
  These bits do not affect the operation.
  DQ_7-DQ_0=04H

  Address (All addresses are the same as the first cycle.)
  A_{20}-A_{16}=Partition address (32M-bit device).
  A_{21}-A_{16}=Partition address (64M-bit or 128M-bit device).
  The partition address must be the address within the partition in which the flash memory interface software is not stored.

A_{15}-A_{11}=Any address.
These bits do not affect the operation.
A_{10}-A_8=Partition configuration register code.
These bits determine the partiton boundaries shown in Table 14 and Figure 15.
A_7-A_0=Any address.
These bits do not affect the operation.

- After writing the second cycle command (04H) and the operation is successfully completed, all the partitions return to the read array mode. If the operation is not completed successfully, the target partition to which the command is written remains in the read status register mode.
- After the second cycle command, write the Read Status Register command (70H) to the partition to which the Set Partition Configuration Register command is written. Then, check the status register of its partition to clarify that the command sequence error is not detected.
- If the command sequence error is detected (SR.5, SR.4="1"), write the Clear Status Register command (50H) to the partition in which the error is detected. After that, reattempt the sequence of setting the partition configuration register.
- If the command sequence error is not detected, write the Read Identifier Codes/OTP command (90H) to the partition to which the Set Partition Configuration Register command is written. Subsequent read operations at the following address output the partition configuration register code.
  A_{20}-A_{16}=Partition address (32M-bit device).
  A_{21}-A_{16}=Partition address (64M-bit or 128M-bit device).
  The partition address must be the address within the partition to which the Read Identifier Codes/ OTP command is written.
  A_{15}-A_0=0006H
- Check the partition configuration register code on the data bus DQ_{10}-DQ_8 to clarify that the partition boundaries are correctly set.
- If the partition boundaries are not set correctly, reattempt the sequence of setting the partition configuration register.

4.17.2 Partition Configuration

The partition configuration shown in Table 14 determines the partiton boundaries for the dual work (simultaneous read while erase/program) operation. The partition boundaries can be set to any plane boundaries. If the partition configuration register bits PCR.10-8 (PC.2-0) are set to "001", the partition boundary is set between plane0 and plane1. There are two partitions in this configuration. Plane1-3 are merged to one partition. Status registers for plane1-3 are also merged to one. If the partition configuration register bits are set to "101", the partition boundaries are set between plane0 and plane1 and between plane2 and plane3. There are three partitions in this configuration. Plane1-2 are merged to one partition. If the partition configuration register bits are set to "111", there are four partitions. Figure 15 illustrates the various partition configuration.

Table 14. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See Figure 15 for the detail on partition configuration.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

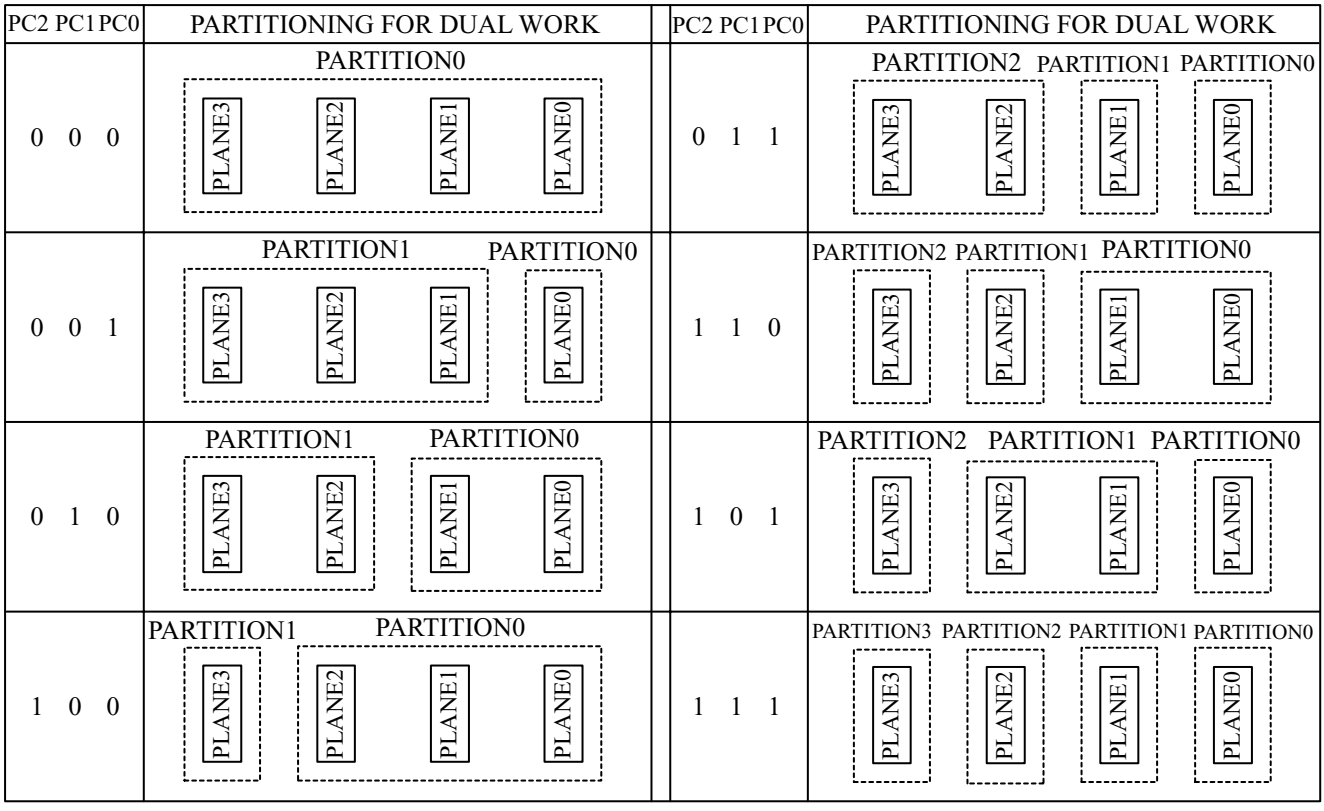
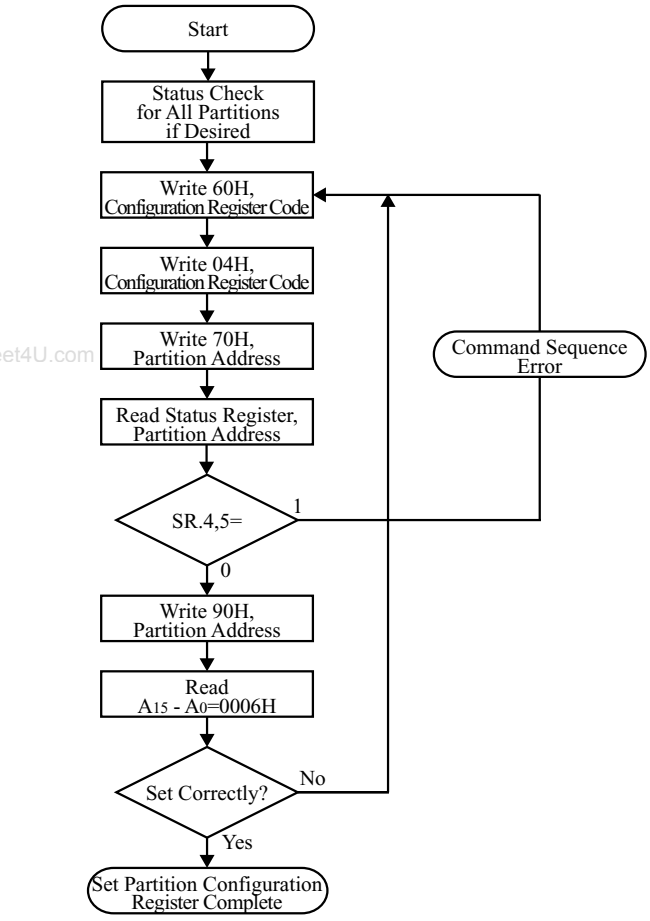
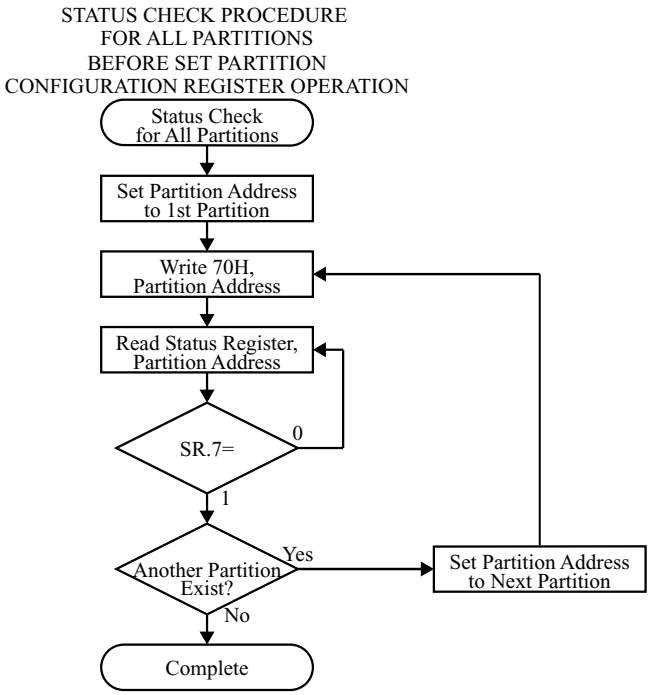


Figure 15. Partition Configuration



Bus Operation	Command	Comments
Write	Set Partition Configuration Register	<First cycle> Data=60H Addr=Partition Configuration Register Code (see Table 14)
		<Second cycle> Data= 04H Addr=Partition Configuration Register Code (see Table 14)
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Partition Configuration Register Code Addr=0006H (see Table 6 through Table 8)
Standby		Check DQ_{10}-DQ_8 for Partition Configuration Register Code
Partition configuration register code can be read after set partition configuration register operation. SR.5 and SR.4 are only cleared by the Clear Status Register command. If an error is detected, clear the status register before attempting retry or other error recovery. After a successful set partition configuration register operation, the device returns to read array mode.		



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 16. Set Partition Configuration Register Flowchart

5 Design Considerations

5.1 Hardware Design Considerations

5.1.1 Control using RST#, CE# and OE#

The device will often be used in large memory arrays. SHARP provides three control input pins to accommodate multiple memory connection. Three control input pins, RST#, CE# and OE# provide for:

- Minimize the power consumption of the memory
- Avoid data confliction on the data bus

To effectively use these control input pins, access the desired memory by enabling the CE# through the address decoder. Connect OE# to READ# control signal of all memory devices and system. With these connections, the selected memory devices are activated and deselected memory devices are in standby mode. RST# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should toggle (once set to V_{IL}) during system reset.

5.1.2 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling for eliminating noises to the system power lines. System designers should consider standby current levels (I_{CCS}), active current levels (I_{CCR}) and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1µF ceramic capacitor connected between each V_{CC}, V_{CCQ} and GND and between V_{PP} and GND (when V_{PP} is used as 12V supply). These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. These capacitors will overcome voltage slumps caused by circuit board trace inductance.

5.1.3 V_{PP} Traces on Printed Circuit Boards

The V_{PP} pin on the product is only used to monitor the power supply voltage and is not used for a power supply pin except for 12V supply. Therefore, even when on-board writing to the flash memory on the system, it is not required to consider that V_{PP} supplies the currents on the printed circuit boards.

However, in erase or program operations with applying 12V±0.3V to V_{PP} pin, V_{PP} is used for the power supply pin. When executing these operations, V_{PP} trace widths and layout should be similar to that of V_{CC} to supply the flash memory cells current for erasing or programming. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

5.1.4 V_{CC}, V_{PP}, RST# Transitions

If V_{PP} is lower than V_{PPLK}, V_{CC} is lower than V_{LKO}, or RST# is not at V_{IH}, block erase, full chip erase, (page buffer) program and OTP program operation are not guaranteed. When V_{PP} error is detected, the status register bits SR.5 or SR.4 (depending on the attempted operation) and SR.3 will be set to "1". If RST# transitions to V_{IL} during the block erase, full chip erase, (page buffer) program or OTP program operation, the status register bit SR.7 will remain "0" until reset operation has been completed. Then, the attempted operation will be aborted and the device will enter reset mode after the completion of the reset sequence. If RST# is taken V_{IL} during a block erase, full chip erase, (page buffer) program or OTP program operation, the memory contents at the aborted location are no longer valid. Therefore, the proper command must be written again after RST# is driven V_{IH}. And also, if V_{CC} transitions to lower than V_{LKO} during a block erase, full chip erase, (page buffer) program or OTP program operation, the attempted operation will be aborted and the memory contents at the aborted location are no longer valid. Write the proper command again after V_{CC} transitions above V_{LKO}.

5.1.5 Power-Up/Down Protection

The product is designed to offer protection against accidental block erase, full chip erase, (page buffer) program, OTP program due to noises during power transitions. When the device power-up, holding V_{PP} and RST# to GND until V_{CC} has reached the specified level and in stable. For additional information, please refer to the AP-007-SW-E *RST#, V_{PP} Electric Potential Switching Circuit*. After power-up, the product defaults to the mode described in Section 2.1.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} voltages are above V_{PPLK}, by referring to Section 5.3 and the following design considerations. Since both CE# and WE# must be at V_{IL} for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection because alternation of memory contents can only occur after successful completion of the two-step command sequences.

The individual block locking scheme, which enables each block to be independently locked, unlocked or locked-down, prevents the accidental data alternation. The device is also disabled until RST# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset during power-up/down, invalid bus conditions can be masked, providing yet another level of memory protection.

5.1.6 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. The nonvolatility of the product increases usable battery life because data is retained when system power is removed.

5.1.7 Automatic Power Savings

Automatic Power Savings (APS) provides low-power operation during active mode. APS mode allows the flash memory to put itself into a low current state when not being accessed. After data is read from the memory array and addresses not switching, the device enters the APS mode where typical I_{CC} current is comparable to I_{CCS}. The flash memory stays in this static state with outputs valid until a new location is read. Standard address access timings (t_{AVQV}) provide new data when addresses are changed. During dual work operation (one partition being erased or programmed, while other partitions are one of read modes), the device cannot enter the APS mode even if the input address remains unchanged.

5.1.8 Reset Operation

During power-up/down or transitions of power supply voltage, hold the RST# pin at V_{IL} to protect data against noises which are caused by invalid bus conditions and initialize the internal circuitry in flash memory. Bringing RST# to V_{IL} resets the internal WSM (Write State Machine) and sets the status register to 80H.

After return from reset, a time t_{PHQV} is required until outputs are valid, and a delay, t_{PHWL} and t_{PHEL}, is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored.

5.2 Software Design Considerations

5.2.1 WSM (Write State Machine) Polling

The status register bit SR.7 provides a software method of detecting block erase, full chip erase, (page buffer) program and OTP program completion. After the Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command is written to the CUI (Command User Interface), SR.7 goes to "0". It will return to "1" when the WSM (Write State Machine) has completed the internal algorithm.

The status register bit SR.7 is "1" state when the device is in the following mode.

- The device can accept the next command.
- Block erase is suspended and (page buffer) program operation is not executed.
- (Page buffer) program is suspended.
- Reset mode

5.2.2 Attention to Program Operation

Do not *re*-program "0" data for the bit in which "0" has been already programmed. This *re*-program operation may generate the bit which cannot be erased.

To change the data from "1" to "0", take the following steps.

- Program "0" for the bit in which you want to change the data from "1" to "0".
- Program "1" for the bit in which "0" has been already programmed.
  (When "1" is programmed, erase/program operations are not executed onto the memory cell in flash memory.)

For example, changing the data from "10111101" to "10111100" requires "11111110" programmed.

5.3 Data Protection Method

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

♦ The below describes data protection method.

1) Protection of data in each block

- Any locked block by setting its block lock bit is protected against the data alternation. When WP# is V_{IL}, any locked-down block by setting its block lock-down bit is protected from lock status changes.
  By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
- For detailed block locking scheme, refer to Sections 4.13 to 4.15.

2) Protection of data with V_{PP} control

- When the level of V_{PP} is lower than V_{PPLK} (V_{PP} lockout voltage), write functions to all blocks including OTP block are disabled. All blocks are locked and the data in the blocks are completely protected.

3) Protection of data with RST#

- Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing RST# to V_{IL}, which inhibits write operation to all blocks including OTP block.
- For detailed description on RST# control, refer to Section 5.1.5.

♦ Protection against noises on WE# signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on WE# signal.

5.4 High Performance Read Mode

This section describes the high performance read mode to increase the read performance. However, the read mode which is available varies according to each product. Refer to the specifications whether the high performance read mode is available or not. The read mode which is not described in the specifications can not be used for that product, even if that read mode is explained in this section.

5.4.1 CPU Compatibility

The product supports high-performance read mode for the parameter and main blocks:

- Asynchronous read mode in which 8-word page mode is available

This read mode provides much higher read accesses than was previously used.

The asynchronous read mode is suitable for non-clocked memory systems and is compatible with standard page-mode ROM. If the system CPU or ASIC does not support page-mode, single asynchronous read modes can be used.

Upon reset, the device defaults to asynchronous read mode and is put into read array mode.

5.4.2 Using Asynchronous Page Mode

After initial power-up or reset mode, the device defaults to asynchronous read mode in which 8-word page mode is available. The asynchronous page mode is available for the parameter and main blocks, and is not supported from other locations within the device, such as the status register, identifier codes, OTP block and query codes. The initial valid address will store 8 words of data in the internal page buffer. Each word is then output onto the data bus by toggling the address A_{2-0}.

The addresses cannot be latched into the device. Therefore, addresses must stay valid throughout the entire read cycle until CE# goes to V_{IH}. Figure 17.1 and Figure 17.2 show a waveform for asynchronous page mode read timing. Note that the address A_{2-0} must be toggled to output the page-mode data.

5.4.3 Single Read Mode

The following data can only be read in single asynchronous read mode.

- Status register
- Query code
- Manufacturer code
- Device code
- Block lock configuration code
- Partition configuration register code
- OTP block

A waveform of read timing for single asynchronous read mode is shown in Figure 18.

Single asynchronous read mode is compatible with previous SHARP flash memory devices. The valid addresses are asserted, and then the device will output data after certain delay time, such as t_{AVQV}, t_{VLQV}, t_{ELQV} or t_{GLQV}. Addresses must stay valid throughout the entire read cycle until CE# goes to V_{IH}.

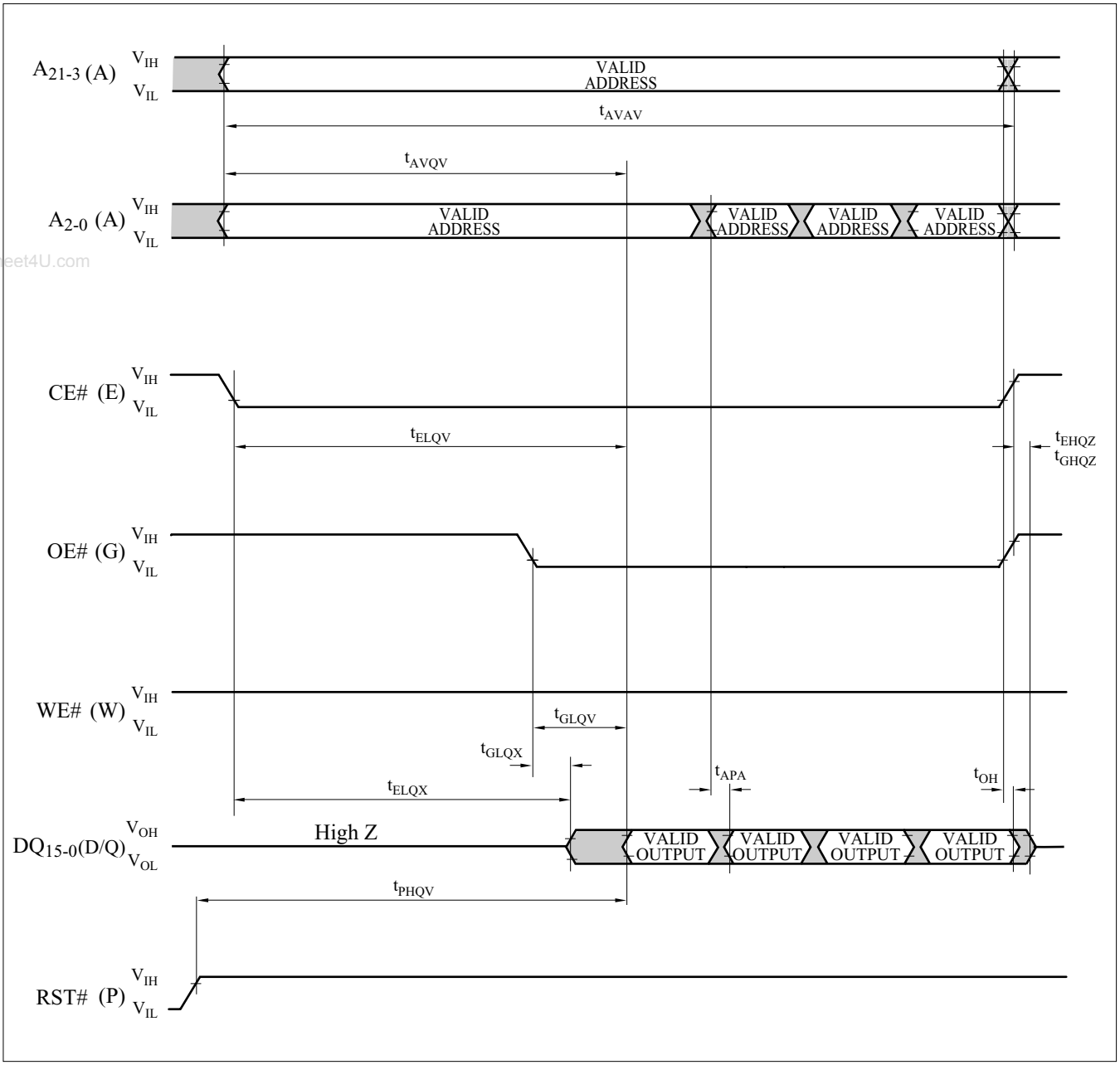


Figure 17.1. AC Waveform for Asynchronous 4-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks
(A_{21} is not used for 32M-bit device.)

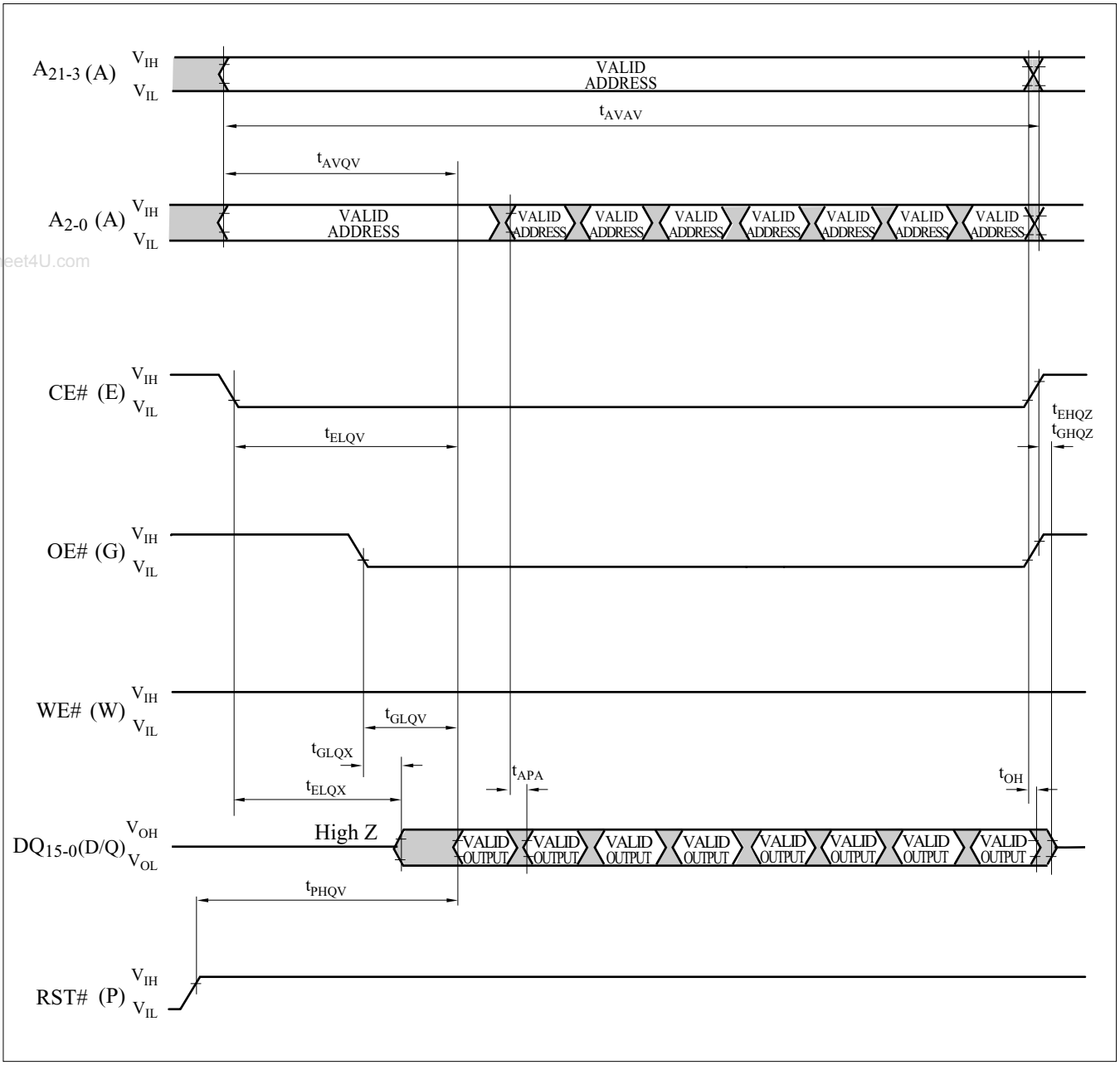


Figure 17.2. AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks (A_{21} is not used for 32M-bit device.)

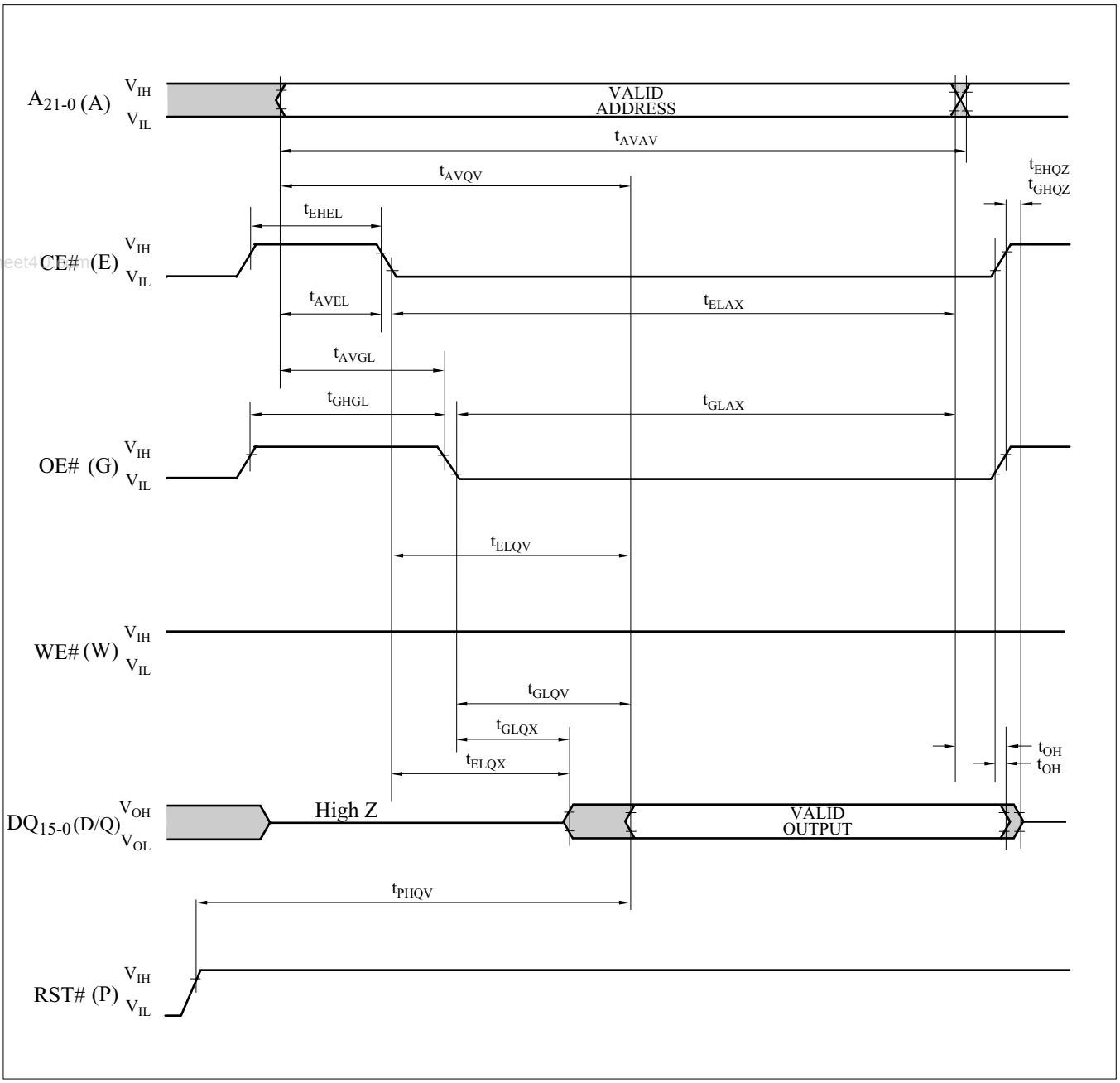


Figure 18. AC Waveform for Single Asynchronous Read Operations
from Status Register, Identifier Codes, OTP Block or Query Code
(A_{21} is not used for 32M-bit device.)

6 Common Flash Interface

This section defines the data structure of the Common Flash Interface (CFI) code, which is called query code. Query code can be read by writing the Read Query command (98H) to the target partition's CUI. System software should confirm this code to gain critical information such as block size, density, bit organization and electrical specifications. Once this code has been obtained, the software will understand which command sets should be used to enable erases, programs and other operations for the flash memory device. The query code is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface or CFI.

6.1 Query Structure Output

The query code allows system software to obtain how to control the flash memory device. The following describes the CFI-compliant interface that allows access to the query code.

.

- The numerical offset value is the address relative to the maximum bus width supported by the device.
- The query table device starting address is a 10H, which is a word address for ×16 devices.
- The query code is presented on the lower-byte data outputs (DQ_{7-0}).
- The device outputs "00H" data on upper byte (DQ_{15-8}) in the read query mode. When verifying the query code information, the upper byte data should be ignored.
- When the query addresses contain two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.
- In all of the following tables, addresses and data are represented in hexadecimal notation, even if the "H" suffix is not noted.
- Some query code data vary according to the device types. Refer to the specifications for the device type to which the product correspond.
- In the case of the product which has two or more BE# (CE#) pins, refer to the query code information of "Device Type" which indicates the same density value as the memory density selected by each BE# (CE#) pin.
- In the case of the product which has 32-bit I/O interface, the query code information of "Device Type" which indicates the value of half a memory density is presented on both lower-word (DQ_{15-0}) and upper-word (DQ_{31-16}) data outputs.

Example of query structure output is shown below.

Table 15. Example of Query Structure Output

Offset	Length	Description	Data	Value
10H	3	Query-unique ASCII string "QRY"	10: 0051H	Q
			11: 0052H	R
			12: 0059H	Y

Offset: Address A_7-A_0 for reading the query code.

A_7-A_0=Offset value shown in the table.

A_{15}-A_8=These bits do not affect the operation.

A_{20}-A_{16}=Partition address (32M-bit device)

A_{21}-A_{16}=Partition address (64M-bit or 128M-bit device)

The partition address must be the address within the partition to which the Read Query command (98H) is written.

Length: Address length of query code.

Each query code information is represented at the addresses from "Offset" to "Offset+Length–1".

Description: Explanation of each query code.

Data: Query code data.

"10: 0051H" means that the read operation at the address A_7-A_0="10H" outputs the data DQ_{15}-DQ_0="0051H".

Value: Meaning of the output data.

6.2 Query Structure Overview

The below table summarized the query structure, which contains the address locations (Offset), the section name and the information for each query code.

Table 16. Query Structure

Offset	Section Name	Information
00H		Manufacturer Code (Refer to Table 6 through Table 8)
01H		Device Code (Refer to Table 6 through Table 8)
(BA+2)H [1]	Block Status Register	Block lock/lock-down information
03H-0FH	Reserved	Reserved for vendor-specific information
10H	CFI Query Identification String	Command set ID and vendor data offset
1BH	System Interface Information	Device voltage and timing information
27H	Device Geometry Definition	Flash device layout information
39H	Sharp-Specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

NOTE:
1. BA = The beginning location of a block address.

6.3 Block Status Register

The Block Status Register indicates whether a target block is locked or locked-down. Block erase, full chip erase or (page buffer) program on the locked block cannot be executed.

The Block Status Register is accessed from Block Base Address (the beginning location of a block address) +2.

Table 17. Block Status Register

Offset	Length	Description	Data	Value
(BA+2)H[1]	1	Block status register bit 0 Block lock status 0 = Unlocked 1 = Locked bit 1 Block lock-down status 0 = Not locked-down 1 = Locked-down bit 2-bit 7 reserved for future use	(BA+2): bit 0=0 or 1 bit 1=0 or 1	See "Description"

NOTE:
1. BA = The beginning location of a block address.

6.4 CFI Query Identification String

The CFI Query Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates that the specification version and supported vendor-specified command set(s).

Table 18. CFI Query Identification String

Offset	Length	Description	Data	Value
10H	3	Query-unique ASCII string "QRY"	10: 0051H	Q
			11: 0052H	R
			12: 0059H	Y
13H	2	Primary vendor command set and control interface ID code 16-bit ID code for vendor-specified algorithms	13: 0003H 14: 0000H	
15H	2	Extended Query Table primary algorithm address	15: 0039H 16: 0000H	39H
17H	2	Alternate vendor command set and control interface ID code 0000H means no second vendor-specified algorithm exists	17: 0000H 18: 0000H	N/A
19H	2	Secondary algorithm Extended Query Table address 0000H means none exists	19: 0000H 1A: 0000H	N/A

6.5 System Interface Information

The following System Interface Information is useful for optimizing the system interface to the flash memory.

Table 19. System Interface Information

Offset	Length	Description	Device Type (1)	Data	Value
1BH	1	Vcc logic supply minimum program/erase voltage bits 0-3 BCD 100mV bits 4-7 BCD volts		1B: 0027H	2.7V
1CH	1	Vcc logic supply maximum program/erase voltage bits 0-3 BCD 100mV bits 4-7 BCD volts	Flash Memory	1C: 0036H	3.6V
			Combination Memory	1C: 0033H	3.3V
1DH	1	Vpp [programming] supply minimum program/erase voltage bits 0-3 BCD 100mV bits 4-7 HEX volts	other than 44SOP	1D: 00B7H	11.7V
			44SOP	1D: 0000H	Vpp pin not provided.
1EH	1	Vpp [programming] supply maximum program/erase voltage bits 0-3 BCD 100mV bits 4-7 HEX volts	other than 44SOP	1E: 00C3H	12.3V
			44SOP	1E: 0000H	Vpp pin not provided.
1FH	1	"n" such that typical single word program time-out = 2^n µs		1F: 0004H	2^4=16µs
20H	1	"n" such that typical max. size buffer write time-out = 2^n µs		20: 0007H	2^7=128µs
21H	1	"n" such that typical block erase time-out = 2^n ms		21: 000AH	2^{10}=1s
22H	1	"n" such that typical full chip erase time-out = 2^n ms	32Mbit	22: 0010H	2^{16}=65.5s
			64Mbit	22: 0011H	2^{17}=131s
23H	1	"n" such that maximum word program time-out = 2^n times typical		23: 0004H	2^4×16µs= 256µs
24H	1	"n" such that maximum max. size buffer write time-out = 2^n times typical		24: 0004H	2^4×128µs= 2048µs
25H	1	"n" such that maximum block erase time-out = 2^n times typical		25: 0003H	2^3×1s= 8s
26H	1	"n" such that maximum full chip erase time-out = 2^n times typical	32Mbit	26: 0003H	2^3×65.5s= 524s
			64Mbit	26: 0003H	2^3×131s= 1048s

NOTE:
1. The query code data varies according to each device type.
   Flash Memory: Flash memory device.
   Combination Memory: Flash memory and SRAM into one package.
   other than 44SOP: The products other than that which is available in 44-lead SOP package.
   44SOP: The product which is available in 44-lead SOP package.
   32Mbit: 32M-bit device.
   64Mbit: 64M-bit device.

6.6 Device Geometry Definition

This section provides the critical details of the flash device geometry.

Table 20.1. Device Geometry Definition

Offset	Length	Description	Device Type (1)	Data	Value
27H	1	"n" such that device size = 2^n in number of bytes	32Mbit	27: 0016H	32Mbit
			64Mbit	27: 0017H	64Mbit
28H	2	Flash device interface ×8: 8-bit data bus (--00H) ×16: 16-bit data bus (0001H) ×8/×16: 8-bit/16-bit data bus (0002H)		28: 0001H 29: 0000H	×16
2AH	2	"n" such that maximum number of bytes in write buffer = 2^n		2A: 0005H 2B: 0000H	16word
2CH	1	Number of erase block regions within device 1. x = 0 means no erase blocking; the device erases in "bulk". 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region. 4. Partition size = (total blocks) × (individual block size)		2C: 0002H	2
2DH	4	Erase Block Region 1 information bits 0-15 = y, y+1 = number of identical-size erase blocks bit 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	2D: 003EH 2E: 0000H 2F: 0000H 30: 0001H	63blocks 32Kwords
			32Mbit, Bottom Parameter	2D: 0007H 2E: 0000H 2F: 0020H 30: 0000H	8blocks 4Kwords
			64Mbit, Top Parameter	2D: 007EH 2E: 0000H 2F: 0000H 30: 0001H	127blocks 32Kwords
			64Mbit, Bottom Parameter	2D: 0007H 2E: 0000H 2F: 0020H 30: 0000H	8blocks 4Kwords

NOTE:
1. The query code data varies according to each device type.
   32Mbit: 32M-bit device.
   64Mbit: 64M-bit device.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.
   64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.

Table 20.2. Device Geometry Definition (Continued)

Offset	Length	Description	Device Type (1)	Data	Value
31H	4	Erase Block Region 2 information bit 0-15 = y, y+1 = number of identical-size erase blocks bit 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	31: 0007H 32: 0000H 33: 0020H 34: 0000H	8blocks 4Kwords
			32Mbit, Bottom Parameter	31: 003EH 32: 0000H 33: 0000H 34: 0001H	63blocks 32Kwords
			64Mbit, Top Parameter	31: 0007H 32: 0000H 33: 0020H 34: 0000H	8blocks 4Kwords
			64Mbit, Bottom Parameter	31: 007EH 32: 0000H 33: 0000H 34: 0001H	127blocks 32Kwords
35H	4	Erase Block Region 3 information bit 0-15 = y; y+1 = number of identical-size erase blocks bit 16-31 = z; region erase block(s) size are z × 256 bytes		35: 0000H 36: 0000H 37: 0000H 38: 0000H	N/A

NOTE:
1. The query code data varies according to each device type.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.
   64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.

6.7 Sharp-Specific Extended Query Table

The vendor-specific extended query tables show the features and commands which are supported in the product.

Table 21. Primary Vendor-Specific Extended Query

Offset	Length	Description	Data	Value
39H	3	Primary Extended Query Table unique ASCII string "PRI"	39: 0050H	P
			3A: 0052H	R
			3B: 0049H	I
3CH	1	Major version number, ASCII	3C: 0031H	1
3DH	1	Minor version number, ASCII	3D: 0033H	3

Table 22.1. Primary Algorithm-Specific Extended Query

Offset	Length	Description	Device Type (1)	Data	Value
3EH	4	Optional feature and command support (1 = yes, 0 = no) bits 10-31 are reserved; undefined bits are "0." If bit 31 is "1" then another 31 bit field of optional features follows at the end of the bit-30 field. bit 0 Chip erase supported bit 1 Suspend erase supported bit 2 Suspend program supported bit 3 Legacy lock/unlock supported bit 4 Queued erase supported bit 5 Instant individual block locking supported bit 6 OTP bits supported bit 7 Page mode read supported bit 8 Synchronous read supported bit 9 Simultaneous operations supported	Page Mode	3E: 00E7H 3F: 0002H 40: 0000H 41: 0000H	bit 0=1 yes bit 1=1 yes bit 2=1 yes bit 3=0 no bit 4=0 no bit 5=1 yes bit 6=1 yes bit 7=1 yes bit 8=0 no bit 9=1 yes
			Single Fixed Partition	3E: 00E7H 3F: 0000H 40: 0000H 41: 0000H	bit 0=1 yes bit 1=1 yes bit 2=1 yes bit 3=0 no bit 4=0 no bit 5=1 yes bit 6=1 yes bit 7=1 yes bit 8=0 no bit 9=0 no

NOTE:

1. The query code data varies according to each device type.
   Page Mode: The device which supports page mode read operations.
   Single Fixed Partition: The device which does not support the flexible partition configuration.
   (For example, the product which is available in 44-lead SOP package.)
   Single partition contains all the blocks. The partition configuration cannot be changed.

Table 22.2. Primary Algorithm-Specific Extended Query (Continued)

Offset	Length	Description	Device Type (1)	Data	Value
42H	1	Supported functions after suspend: read array, status, query Other supported operations are: bits 1-7 are reserved; undefined bits are "0" bit 0 Program supported after erase suspend		42: 0001H	bit 0=1 yes
43H	2	Block status register mask bit 2-15 are reserved; undefined bits are "0" bit 0 Block lock bit status register active bit 1 Block lock-down bit status active		43: 0003H 44: 0000H	bit 0=1 yes bit 1=1 yes
45H	1	Vcc logic supply highest performance program/erase voltage bit 0-3 BCD value in 100mV bit 4-7 BCD value in volts		45: 0030H	3.0V
46H	1	Vpp optimum program/erase supply voltage bits 0-3 BCD value in 100mV bits 4-7 HEX value in volts	$V_{PP}=V_{PPH1}/V_{PPH2}$	46: 00C0H	12.0V
			$V_{PP}=V_{PPH1}$	46: 0030H	3.0V
			44SOP	46: 0000H	Vpp pin not provided.

NOTE:
1. The query code data varies according to each device type.
$V_{PP}=V_{PPH1}/V_{PPH2}$: The device which supports the fast erasing and fast programming mode with applying 12V to V_{PP}.
$V_{PP}=V_{PPH1}$: The device which does not support the fast erasing and fast programming mode.
44SOP: The product which is available in 44-lead SOP package.

Table 23. OTP Block Information

Offset	Length	Description	Data	Value
47H	1	Number of OTP block fields in JEDEC ID space "00H" indicates that 256 protection fields are available	47: 0001H	1
48H	4	OTP Block Field 1: OTP Description This field describes user-available One Time Programmable (OTP) block bytes. Some are pre-programmed with device-unique numbers. Others are user-programmable. Bits 0-15 point to the OTP block lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0-7 = Lock/bytes JEDEC-plane physical low address bits 8-15 = Lock/bytes JEDEC-plane physical high address bits 16-23 = "n" such that 2^n = factory pre-programmed bytes bits 24-31 = "n" such that 2^n = user-programmable bytes	48: 0080H 49: 0000H 4A: 0003H 4B: 0003H	80H 00H 8byte 8byte

Table 24. Burst Read Information

Offset	Length	Description	Device Type (1)	Data	Value
4CH	1	Page mode read capability bits 0-7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28H for device word width to determine the page-mode data output width. 00H indicates no read page buffer.		4C: 0004H	8word
4DH	1	Number of synchronous mode read configuration fields that follow. 00H indicates no burst capability.	Page Mode	4D: 0000H	no
4EH	1	Synchronous mode read capability configuration 1 bits 3-7 are reserved; bits 0-2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07H indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bits 0-2 if the device is configured for its maximum word width. See offset 28H for word width to determine the burst data output width.	Page Mode	4E: 0000H	N/A
4FH	1	Synchronous mode read capability configuration 2	Page Mode	4F: 0000H	N/A
50H	1	Synchronous mode read capability configuration 3	Page Mode	50: 0000H	N/A

NOTE:
1. The query code data varies according to each device type.
Page Mode: The device which supports page mode read operations.

Table 25. Partition Information

Offset	Length	Description	Device Type (1)	Data	Value
51H	1	Number of device hardware-partition regions within the device x = 0: a single hardware partition device (no fields follow) x specifies the number of device partition regions containing one or more contiguous erase block regions (flexible)	Flexible Partition	51: 0002H	2 (2)
			Two Fixed Partitions	51: 0002H	2
			Single Fixed Partition	51: 0000H	0 (3)

NOTES:

1. The query code data varies according to each device type.
   Flexible Partition: The device which supports the flexible partition configuration.
   The partition boundaries can be changed by using the Set Partition Configuration Register command.
   Two Fixed Partitions: The device which does not support the flexible partition configuration.
   The memory array is divided into two partitions and the partition configuration cannot be changed.
   Refer to the specification for the partition boundary.
   Single Fixed Partition: The device which does not support the flexible partition configuration.
   (For example, the product which is available in 44-lead SOP package.)
   Single partition contains all the blocks. The partition configuration cannot be changed.
2. This is the default value after power-up or device reset and until changing the partition configuration.
   Changes of the partition configuration do not affect this value.
   For example, even if the memory array is divided into four partitions by using the Set Partition Configuration Register command, the query code data at the offset "51H" remains "0002H".
3. If the query code data at the offset "51H" is "0000H", subsequent query code data from the offset "52H" to "77H" are all "FFFFH".

Table 26.1. Partition Region 1 Information (Partition and Erase-block Region Information) (1)

Offset	Length	Description	Device Type (2)	Data	Value
52H	2	Number of identical partitions within the partition region		52: 0001H 53: 0000H	1
54H	1	Simultaneous program or erase operations allowed in other partitions while this partition is in read mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		54: 0011H	program: 1 erase: 1 (3)
55H	1	Simultaneous program or erase operations allowed in other partitions while this partition is in program mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		55: 0000H	program: 0 erase: 0
56H	1	Simultaneous program or erase operations allowed in other partitions while this partition is in erase mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		56: 0000H	program: 0 erase: 0
57H	1	Number of erase block regions in this partition region 1. x = 0 = no erase blocking; the partition region erases in "bulk" 2. x specifies the number of erase block regions containing one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) × (individual block size)	Top Parameter	57: 0001H	1
			Bottom Parameter	57: 0002H	2

NOTES:
1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above.
2. The query code data varies according to each device type.
   Top Parameter: The device which contains the parameter blocks at the highest address.
   Bottom Parameter: The device which contains the parameter blocks at the lowest address.
3. Simultaneous program and erase is not allowed.

Table 26.2. Partition Region 1 Information (Partition and Erase-block Region Information) (1) (Continued)

Offset	Length	Description	Device Type (2)	Data	Value
58H	4	Partition Region 1 Erase Block Region 1 information bits 0-15 = y, y+1 = number of identical-size erase blocks bits 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	58: 002FH 59: 0000H 5A: 0000H 5B: 0001H	48blocks 32Kwords
			32Mbit, Bottom Parameter	58: 0007H 59: 0000H 5A: 0020H 5B: 0000H	8blocks 4Kwords
			64Mbit, Top Parameter	58: 005FH 59: 0000H 5A: 0000H 5B: 0001H	96blocks 32Kwords
			64Mbit, Bottom Parameter	58: 0007H 59: 0000H 5A: 0020H 5B: 0000H	8blocks 4Kwords
5CH	2	Partition Region 1 (Erase Block Region 1) minimum block erase cycles × 1000		5C: 0064H 5D: 0000H	100,000 cycles
5EH	1	Partition Region 1 (Erase Block Region 1) bits per cell; internal error correction (ECC) bits 0-3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1 = yes, 0 = no) bits 5-7 = reserved for future use		5E: 0001H	1bit/cell bit 4=0 no
5FH	1	Partition Region 1 (Erase Block Region 1) page mode and synchronous mode capabilities as defined in "Burst Read Information" bit 0 = page mode host reads permitted (1 = yes, 0 = no) bit 1 = synchronous host reads permitted (1 = yes, 0 = no) bit 2 = synchronous host writes permitted (1 = yes, 0 = no) bits 3-7 = reserved for future use	Page Mode	5F: 0001H	bit 0=1 yes bit 1=0 no bit 2=0 no

NOTES:
1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above. For example, after the memory array of 32M-bit device is divided into four partitions by using the Set Partition Configuration Register command, the number of 32K-word blocks in one partition are 15 or 16 blocks. However, the query code data at the offset "58H" remains unchanged.
2. The query code data varies according to each device type.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.
   64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.
   Page Mode: The device which supports page mode read operations.

Table 26.3. Partition Region 1 Information (Partition and Erase-block Region Information) (1) (Continued)

Offset (2)	Length	Description	Device Type (3)	Data	Value
60H (Bottom)	4	(information for bottom parameter device) Partition Region 1 Erase Block Region 2 information bits 0-15 = y, y+1 = number of identical-size erase blocks bits 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	N/A	N/A
			32Mbit, Bottom Parameter	60: 000EH 61: 0000H 62: 0000H 63: 0001H	15blocks 32Kwords
			64Mbit, Top Parameter	N/A	N/A
			64Mbit, Bottom Parameter	60: 001EH 61: 0000H 62: 0000H 63: 0001H	31blocks 32Kwords
64H (Bottom)	2	(information for bottom parameter device) Partition Region 1 (Erase Block Region 2) minimum block erase cycles × 1000	Top Parameter	N/A	N/A
			Bottom Parameter	64: 0064H 65: 0000H	100,000 cycles
66H (Bottom)	1	(information for bottom parameter device) Partition Region 1 (Erase Block Region 2) bits per cell; internal error correction (ECC) bits 0-3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1 = yes, 0 = no) bits 5-7 = reserved for future use	Top Parameter	N/A	N/A
			Bottom Parameter	66: 0001H	1bit/cell bit 4=0 no
67H (Bottom)	1	(information for bottom parameter device) Partition Region 1 (Erase Block Region 2) page mode and synchronous mode capabilities defined in "Burst Read Information" bit 0 = page mode host reads permitted (1 = yes, 0 = no) bit 1 = synchronous host reads permitted (1 = yes, 0 = no) bit 2 = synchronous host writes permitted (1 = yes, 0 = no) bits 3-7 = reserved for future use	Page Mode, Top Parameter	N/A	N/A
			Page Mode, Bottom Parameter	67: 0001H	bit 0=1 yes bit 1=0 no bit 2=0 no

NOTES:
1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above.
   For example, after the memory array of 32M-bit device is divided into two partitions in which each partition has 16M-bit density by using the Set Partition Configuration Register command, the number of 32K-word blocks in each partition are 31 or 32 blocks. However, the query code data at the offset "60H" remains unchanged.
2. The notation (Bottom) in "Offset" means that offset addresses are applicable to only bottom parameter device. Refer to "Partition Region 2 Information" for offset addresses from "60H" to "67H" of the top parameter device.
3. The query code data varies according to each device type.
   Top Parameter: The device which contains the parameter blocks at the highest address.
   Bottom Parameter: The device which contains the parameter blocks at the lowest address.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.
   64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.

Page Mode, Top Parameter: The device which supports page mode read operations and contains the parameter blocks at the highest address.
Page Mode, Bottom Parameter: The device which supports page mode read operations and contains the parameter blocks at the lowest address.

Table 27.1. Partition Region 2 Information (Partition and Erase-block Region Information) (1)

Offset (2)	Length	Description	Device Type (3)	Data	Value
60H (Top)	2	Number of identical partitions within the partition region		60: 0001H 61: 0000H	1
68H (Bottom)				68: 0001H 69: 0000H	
62H (Top)	1	Simultaneous program or erase operations allowed in other partitions while this partition is in read mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		62: 0011H	program: 1 erase: 1 (4)
6AH (Bottom)				6A: 0011H	
63H (Top)	1	Simultaneous program or erase operations allowed in other partitions while this partition is in program mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		63: 0000H	program: 0 erase: 0
6BH (Bottom)				6B: 0000H	
64H (Top)	1	Simultaneous program or erase operations allowed in other partitions while this partition is in erase mode bits 0-3 = number of simultaneous program operations bits 4-7 = number of simultaneous erase operations		64: 0000H	program: 0 erase: 0
6CH (Bottom)				6C: 0000H	
65H (Top)	1	Number of erase block regions in this partition region 1. x = 0 = no erase blocking; the partition region erases in "bulk" 2. x specifies the number of erase block regions containing one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) × (individual block size)	Top Parameter	65: 0002H	2
6DH (Bottom)			Bottom Parameter	6D: 0001H	1

NOTES:
1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above.
2. The notation (Top) in "Offset" means that offset addresses are applicable to top parameter device. The notation (Bottom) in "Offset" means that offset addresses are applicable to bottom parameter device.
3. The query code data varies according to each device type. Top Parameter: The device which contains the parameter blocks at the highest address. Bottom Parameter: The device which contains the parameter blocks at the lowest address.
4. Simultaneous program and erase is not allowed.

Table 27.2. Partition Region 2 Information (Partition and Erase-block Region Information) (1) (Continued)

Offset (2)	Length	Description	Device Type (3)	Data	Value
66H (Top)	4	Partition Region 2 Erase Block Region 1 information bits 0-15 = y, y+1 = number of identical-size erase blocks bits 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	66: 000EH 67: 0000H 68: 0000H 69: 0001H	15blocks 32Kwords
6EH (Bottom)			32Mbit, Bottom Parameter	6E: 002FH 6F: 0000H 70: 0000H 71: 0001H	48blocks 32Kwords
66H (Top)			64Mbit, Top Parameter	66: 001EH 67: 0000H 68: 0000H 69: 0001H	31blocks 32Kwords
6EH (Bottom)			64Mbit, Bottom Parameter	6E: 005FH 6F: 0000H 70: 0000H 71: 0001H	96blocks 32Kwords
6AH (Top)	2	Partition Region 2 (Erase Block Region 1) minimum block erase cycles × 1000	Top Parameter	6A: 0064H 6B: 0000H	100,000 cycles
72H (Bottom)			Bottom Parameter	72: 0064H 73: 0000H	100,000 cycles
6CH (Top)	1	Partition Region 2 (Erase Block Region 1) bits per cell; internal error correction (ECC) bits 0-3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1 = yes, 0 = no) bits 5-7 = reserved for future use	Top Parameter	6C: 0001H	1bit/cell bit 4=0 no
74H (Bottom)			Bottom Parameter	74: 0001H	1bit/cell bit 4=0 no
6DH (Top)	1	Partition Region 2 (Erase Block Region 1) page mode and synchronous mode capabilities as defined in "Burst Read information" bit 0 = page mode host reads permitted (1 = yes, 0 = no) bit 1 = synchronous host reads permitted (1 = yes, 0 = no) bit 2 = synchronous host writes permitted (1 = yes, 0 = no) bits 3-7 = reserved for future use	Page Mode, Top Parameter	6D: 0001H	bit 0=1 yes bit 1=0 no bit 2=0 no
75H (Bottom)			Page Mode, Bottom Parameter	75: 0001H	bit 0=1 yes bit 1=0 no bit 2=0 no

NOTES:

1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above.
   For example, after the memory array of 32M-bit device is divided into two partitions in which each partition has 16M-bit density by using the Set Partition Configuration Register command, the number of 32K-word blocks in each partition are 31 or 32 blocks. However, the query code data at the offset "66H" remains unchanged.
2. The notation (Top) in "Offset" means that offset addresses are applicable to top parameter device.
   The notation (Bottom) in "Offset" means that offset addresses are applicable to bottom parameter device.
3. The query code data varies according to each device type.
   Top Parameter: The device which contains the parameter blocks at the highest address.
   Bottom Parameter: The device which contains the parameter blocks at the lowest address.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.

64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.
Page Mode, Top Parameter: The device which supports page mode read operations and contains the parameter blocks at the highest address.
Page Mode, Bottom Parameter: The device which supports page mode read operations and contains the parameter blocks at the lowest address.

Table 27.3. Partition Region 2 Information (Partition and Erase-block Region Information) (1) (Continued)

Offset (2)	Length	Description	Device Type (3)	Data	Value
6EH (Top)	4	(information for top parameter device) Partition Region 2 Erase Block Region 2 information bits 0-15 = y, y+1 = number of identical-size erase blocks bits 16-31 = z, region erase block(s) size are z × 256 bytes	32Mbit, Top Parameter	6E: 0007H 6F: 0000H 70: 0020H 71: 0000H	8blocks 4Kwords
			32Mbit, Bottom Parameter	N/A	N/A
			64Mbit, Top Parameter	6E: 0007H 6F: 0000H 70: 0020H 71: 0000H	8blocks 4Kwords
			64Mbit, Bottom Parameter	N/A	N/A
72H (Top)	2	(information for top parameter device) Partition Region 2 (Erase Block Region 2) minimum block erase cycles × 1000	Top Parameter	72: 0064H 73: 0000H	100,000 cycles
			Bottom Parameter	N/A	N/A
74H (Top)	1	(information for top parameter device) Partition Region 2 (Erase Block Region 2) bits per cell; internal error correction (ECC) bits 0-3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1 = yes, 0 = no) bits 5-7 = reserved for future use	Top Parameter	74: 0001H	1bit/cell bit 4=0 no
			Bottom Parameter	N/A	N/A
75H (Top)	1	(information for top parameter device) Partition Region 2 (Erase Block Region 2) page mode and synchronous mode capabilities defined in "Burst Read Information" bit 0 = page mode host reads permitted (1 = yes, 0 = no) bit 1 = synchronous host reads permitted (1 = yes, 0 = no) bit 2 = synchronous host writes permitted (1 = yes, 0 = no) bits 3-7 = reserved for future use	Page Mode, Top Parameter	75: 0001H	bit 0=1 yes bit 1=0 no bit 2=0 no
			Page Mode, Bottom Parameter	N/A	N/A
76H	1	Features space definitions (reserved for future use)		76: FFFFH	reserved
77H		Reserved for future use		77: FFFFH	reserved

NOTES:
1. This table shows the default informations after power-up or device reset and until changing the partition configuration. Changes of the partition configuration do not affect the query code data shown above.
2. The notation (Top) in "Offset" means that offset addresses are applicable to only top parameter device. Refer to previous page for offset addresses from "6EH" to "75H" of the bottom parameter device.
3. The query code data varies according to each device type.
   Top Parameter: The device which contains the parameter blocks at the highest address.
   Bottom Parameter: The device which contains the parameter blocks at the lowest address.
   32Mbit, Top Parameter: 32M-bit device which contains the parameter blocks at the highest address.
   32Mbit, Bottom Parameter: 32M-bit device which contains the parameter blocks at the lowest address.
   64Mbit, Top Parameter: 64M-bit device which contains the parameter blocks at the highest address.
   64Mbit, Bottom Parameter: 64M-bit device which contains the parameter blocks at the lowest address.

Page Mode, Top Parameter: The device which supports page mode read operations and contains the parameter blocks at the highest address.
Page Mode, Bottom Parameter: The device which supports page mode read operations and contains the parameter blocks at the lowest address.

7 Related Document Information(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-003-CFI-E	Common Flash memory Interface Specification
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.