EZFA cart internals (256M model).

2 * AM29LV128ML (NOR FLASH chips)

1 * 512Kbyte SRAM (Don't care about model, battery backed-up)

1 * Unknown CPLD (Don't care)

1 * Unknown RTC (Care, but no info)

CPLD internal registers

Name	Address	Usage
EZFA_ACC_REG	0x09FFFFFE	Access register
EZFA_CNT_REG	0x09FFFFFC	Control register
EZFA_ROM_REG	0x09FFFFFA	ROM offset register
EZFA_RAM_REG	0x09FFFFF8	RAM bank register

Enable access to internal registers

Register	Value (x16)
EZFA_ACC_REG	0x5959

Disable access to internal registers

Register	Value (x16)
EZFA_ACC_REG	0x0000

Control register (EZFA_CNT_REG)

Bit	Meaning
0	Enable write access to FLASH chips
1	Enable write access to ROM offset register
2	Enable write access to RAM bank register
3	Enable write access to backup SRAM chip

ROM offset register (EZFA_ROM_REG) (x16, all bits used)

Translates 0x08000000 <= (EZFA_ROM_REG << 3) + 0x08000000

RAM bank register (EZFA_ROM_REG) (x16, lower 3 bits used)

Controls the upper 3 address lines of SRAM (A16, A17, A18)

Made by Pavel Ionut. Thank you Martin Korth for GBATEK!